Behavioral modeling and simulation of digital phase-locked loops using VHDL-AMS

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This paper presents a simulation VHDL-AMS – based model of digital phase-locked loop – PLL (DPLL) for mixed-signal applications. The described model is of behavioral type, which ensures in a large extend its versatility. The created model is developed as a hierarchical design using hierarchical blocks to represent the basic elements of the monolithic DPLL. It is built of block that simulates the behavior of the digital phase detector (PD), low-pass filter (LPF), voltage-controlled oscillator (VCO) and programmable frequency divider. The modeling of the DPLL behavior is implemented and corresponds to the format of the simulation software System Vision 5.5 (from Mentor Graphics). The model parameters are extracted for the monolithic PLL CD74HC4046 from Texas Instruments as an example. Confirmation of the validity of the proposed model is made by comparison of the simulation results, manufacturer's data and the results of the experimental study of the breadboard circuits with 4046. This results in good agreement between simulations and performance of the actual devices (the maximum error is not higher than 10%).

Поведенческо моделиране и симулация на цифрови фазово затворени вериги, използвайки VHDL-AMS (Мариета Ковачева). *В тази статия е представен поведенчески VHDL-AMS модел на цифрова фазово затворена верига – PLL (DPLL). Описаният в статията модел е от поведенчески тип, чрез което се осигурява с голяма степен неговата универсалност. Моделът е създаден като йерархична структура от блокове отразяващи поведението на базовите елементи на монолитните DPLL схеми. Той е изграден от блокове, симулиращи поведението на цифров фазов детектор, нискочестотен филтър (НЧФ), генератор, управляван от напрежение (ГУН) и програмируем делител на честота. Моделирането на поведението на DPLL е изпълнено и отговаря на формата на симулационната програма System Vision 5.5 (част от програмната система Mentor Graphics). Моделните параметри са определени за монолитния PLL CD74HC4046, използвани като пример в статията. Валидацията на модела е изпълнена чрез сравнение на симулационните резултати с типичните стойности на основните параметри от каталожните данни и с резултати от експериментално изследване на опитни схеми с 4046. Анализът на получените резултати показа добро покритие между компютърните симулации и поведението на реалните интегрални схеми (максималната стойност на относителната грешка не надвишава 10%).*

Introduction

The digital phase-locked loops – PLLs (DPLLs) are feedback mixed-signal systems that include mainly a voltage-controlled oscillator (VCO), phase-frequency detector (PFD), and low-pass filter (LPF) within their loop. For the DPLL the frequency of the generated clock signal has to be synchronized (or locked) with the frequency of an external input digital signal [1], [2], [3], [4]. The DPLL systems are widely used in the measurement systems and telecommunications and are used for building of frequency synthesizers, synchronizers, FM demodulators, decoders, etc [3], [5]. Therefore of particular interest is the creation of simulation models suitable for computer based analysis and design of electronic systems containing such type mixed-signal circuits.

In the recent ten years, a number of papers have been published describing various simulation models for PLLs [6]-[10]. For example, in [6] a structure of VHDL-AMS model of a dual PLL based frequency synthesizer is shown and two behavioral models of VCOs are presented suitable for sinusoidal signals. Moreover, in [6] the library model chosen for a PD is a simple EXOR gate. This is a purely digital VHDL model. ADC and DAC are used as converters at the

interfaces. In [7] is proposed method for creating models for PLL integrated circuits, such as the analog phase detector structures, representing analog multiplier. The PLL model, given in [8], uses a digital phase detector for random input signals [1], but the input and output signals are periodic signals with a sinusoidal waveform. In [9] is presented Simulink RF Toolbox – based model of the PLL circuit for multi-wireless applications. In this model the structure and the parameters are optimized for implementation on specialized ICs with specific technology that do not match with those used in electronic equipment monolithic PLLs. In 2011, in Ref. [10] a very accurate model of the PLL circuit is presented, built as a transistor-level electronic circuit (*device-* (*transistor-*) *level model*), but with relatively complex topological and parametric structure and applicable for TSMC 65nm CMOS technology.

Testing a complete mixed-signal system via transistor-level simulation is an extremely difficult process and can often become infeasible due to the limitation of simulation capacity. A similar difficulty is encountered when high-level design is performed for the whole system. One method to decrease simulation time and improve the convergence, without a significant loss of information, is by using behavioral modeling technique. Nowadays one of the most effective techniques for behavioral modeling of analog and mixed-signal electronic circuits is by using VHDL-AMS [11], [12].

The aim of this work is to create a VHDL-AMS model of monolithic digital PLL ICs and to use the model for simulation of PLLs main electrical characteristics. Therefore a frequency synthesizer was created using clock divider with random division factor.

Principle of DPLL operation

In general the PLLs are mixed-signal electronic systems which generate a clock output signal which is locked or synchronized with the external input signal. It is possible to have a constant value of the phase shift ϕ_0 between the input signal and clock output signal, but when locked, the frequencies must exactly track, i.e.:

(1) $\phi_{out}(t) = \phi_{in}(t) + \phi_0$ and

(2) $\omega_{out}(t) = \omega_{in}(t)$.

The PD of the PLL circuits compares the phase at each input and generates a signal U_ϕ proportional to the phase difference between the clock output signal and the external input signal.

(3) $U_\phi(t) = K_D[\phi_{out}(t) - \phi_{in}(t)]$,

where K_D is the PD gain in *V/radians*.

The output voltage U_ϕ of the PD is filtered by LPF, removing the high frequency harmonics. Actually, the LPF determines the average value of the U_ϕ. To ensure sufficient stability of the PLL most commonly is used first-order LPF with one pole-zero pair [1], [4]. Thus, for high frequencies the slope of the complete phase transfer function is reduced to $-20dB/dec$, while the phase margin becomes more than 45°.

The frequency of the VCO in the PLLs can be varied by means of the control voltage U_f, obtained by the LPF, according to the following general formula

(4) $f_{out} = f_0 + K_0 U_f$,

where K_0 is the VCO gain in Hz/V and f_0 is the VCO centre frequency.

The DPLLs allow a faster lock time to be achieved and are very suitable for clock generation on high performance microprocessors. An object of analysis and modeling in this paper are the DPLLs, employing phase frequency detector (PFD) with tri-state output.

A basic block diagram of a DPLL using PFD with tri-state output is shown on Fig. 1. In locked state for low frequencies the equivalent phase transfer function is [2]-[5]:

(5) $$T(p) = \frac{K_0 K_D K_N T_{LP}(p)}{p + K_0 K_D K_N T_{LP}(p)} = \frac{K.T_{LP}(p)}{p + K.T_{LP}(p)},$$

where $K = K_0 K_D K_N$ is the gain of the loop network, $T_{LP}(p) = \frac{1 + p\tau_2}{1 + p(\tau_1 + \tau_2)}$ ($\tau_1 = R_1 C$ and $\tau_2 = R_2 C$) is the transfer function of the LPF with one pole-zero pair.

The parameter K_N of the divider, connected within negative feedback of the DPLL is equal to $1/N$ (N is the feedback loop division factor).

After substituting the formula for the transfer function of the LPF into (5) for the phase transfer

function of the DPLL is found

$$(6) \qquad T(p) = \frac{K(1+p\tau_2)/(\tau_1+\tau_2)}{p^2 + p(1+K\tau_2)/(\tau_1+\tau_2) + k/(\tau_1+\tau_2)} = \frac{p(2\xi\omega_n - \omega_n^2/K) + \omega_n^2}{p^2 + 2\xi\omega_n p + \omega_n^2}.$$

After comparison of the left and right sides of the above equation for the following formulas was obtained: $\omega_n = \sqrt{K/(\tau_1+\tau_2)}$ – natural frequency and $\xi = \frac{\omega_n}{2}(\tau_2 + 1/K) \approx \frac{\omega_n}{2}\tau_2$ – damping factor.

Therefore, the lock frequency range of the DPLL is given by

$$(7) \qquad \Delta\omega_L \approx 4\pi\xi\omega_n .$$

and the capture range is $\Delta f_C \approx \xi\omega_n/\pi$. Higher natural frequency ω_n determined wider capture range.

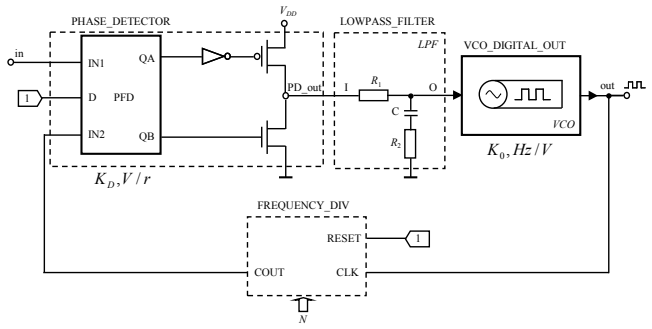

Fig. 1. Block diagram of a DPLL using a sequential PFD.

Modeling of DPLL using VHDL-AMS

The technical requirement for effective models is generally fulfilled when the simplest possible model is developed. The simple models have a number of advantages. They can be developed faster, are more flexible, require less data, run faster and the results are easier to interpret, since the structure of the model is better understood. When the complexity increases, these advantages are lost. The proposed behavioral model of the DPLL is developed following the design method based on a Top-Down analysis approach [13] and applying techniques known from macromodeling of analog integrated circuits [14]. The process of model building and testing can be divided into three main steps: 1) structure the model, 2) build the model and 3) validate the model.

The VHDL-AMS language

The VHDL-AMS (Very High Speed Integrated Circuit Hardware Description Language – Analog and Mixed-Signal), an IEEE standard 1076.1, is an extension of VHDL hardware description language, which is used for description and simulation of event-driven systems [11] [12]. VHDL-AMS purpose is to support the description and the simulation of analog and mixed signal circuits and systems. On the mixed-signal side, a variety of abstraction levels are supported. The VHDL-AMS modeling is not restricted to mixed-signal applications but also supports thermal, mechatronic, optical and other systems.

The model description

The proposed behavioral model is composed on the basis of the block structure of the DPLL circuit shown on Fig. 1. It is assumed that when in capture and lock modes of operation the PLL circuit is a linear electronic system.

The block diagram of the model, whose elements are represented as hierarchical blocks, corresponds to the circuit on Fig. 1. The model parameter values are set to the defaults to ensure the right simulation process. In the process of modeling of specific integrated circuit the model parameters are user defined based on the principle of operation and the manufacturer's data.

A. A hierarchical block for modeling of the VCO

For the VCO model a vco_digital_out element is used (Fig. 2). This element is a series connection of analog VCO – vcoanalog and comparator with digital output – comparator_d by the Mentor Graphics VHDL-AMS open source model library [15]. It has an input analog terminal of type electrical and output digital port of type std_logic. The VCO model is with differential input and output. Formed by the LPF dc voltage is passed to the non-inverting input *in_p* of the VCO. The inverting input *in_n* is referred to ground.

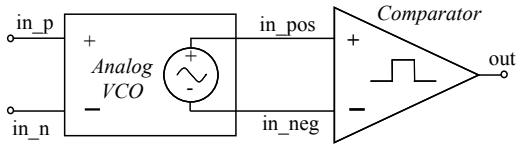

Fig. 2. Block diagram of a VCO with digital output.

The output frequency of the generated output sinusoidal signal is determined by the formula

$$(8) \qquad Fout = F0 + K0(vtmp - Vc),$$

where *vtmp* is the input controlled voltage and *Vc* is input voltage that gives *F0.*

If the input voltage *vtmp* is equal to *Vc* the frequency of the output signal is equal to *F0*.

The symmetrical sinusoidal signal is formed on the

analog VCO output. This signal is passed to a comparator with analog inputs *in_pos* and *in_neg* and digital output *out*. The comparator detects threshold crossing and assigns event on the output.

B. A hierarchical block for modeling of the PFD

The equivalent circuit of the block PFD is shown on Fig. 3. The PFD consist of two edge-triggered D flip-flops, one NAND gate for subtraction of the signals QA and QB, two NOR elements, three inverters and an output stage, which is composed of a complementary pair of MOS transistors (CMOS). The elements bordered by a dashed line as a behavioral VHDL-AMS model are presented (Fig. 4).

The CMOS transistors of the output stage are represented by SPICE models built into the standard library of simulation software system SystemVision (from Mentor Graphics). The model parameters of the MOS transistors are with the default values.

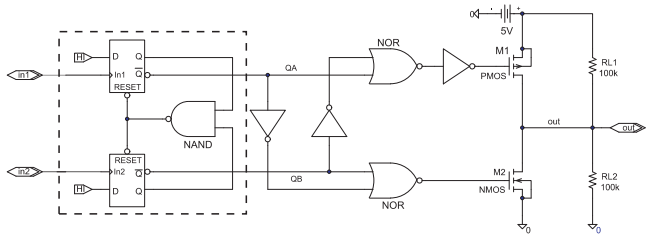

Fig. 3. An equivalent circuit of the PFD model.

The duration of the output pulse is equal to the time interval the positive-going zero crossing of in1 and those of in2. Hence, the mean value of the output voltage is

$$(9) \qquad U_{out} = V_{CC}\frac{\Delta t}{T} = V_{CC}\frac{\varphi}{4\pi}.$$

Moreover the phase shift (within a range $\pm 360°$) is proportional to the duration of the output impulse. Based on the formula (9) for the sensitivity of the phase detector is obtained

$$(10) \qquad k_d = V_{CC}/4\pi.$$

```
library ieee;
use ieee.std_logic_1164.all;
    entity PD is
       port( D,In1,In2 :in STD_LOGIC; QB :out STD_LOGIC;
    QA :out STD_LOGIC);
    end entity PD;
architecture arch_pd of PHASE_DETECTOR is
    signal  QA : STD_LOGIC :='0';
    signal  QB : STD_LOGIC:='0';
    signal  reset : STD_LOGIC:='0';
begin
reset <=  QoutA nand QoutB ;
data_in1 : process(In1, reset) is -- process 1
    begin
   if In1 = '1' and In1'event then
      QoutA <=  '1' ;
      QA <= '0';
   elsif reset = '0' then
     QoutA <=  '0' ;
     QA <= '1';
    end if;
end process data_in1;
--… process 2
……
end architecture arch_pd;
```

Fig. 4. A part of the PFD behavioral VHDL-AMS model.

C. A hierarchical block for modeling of the LPF

The block for modeling the LPF implements the following transfer function

$$(11) \qquad H(p) = H_0[(1+p.tau2)/(1+p.tau1)],$$

where H_0 is the pass-band gain, a $tau1$ $[s]$ and $tau2$ $[s]$ are the time constants of the denominator and nominator, respectively.

Based on this transfer function is constructed the block LOWPASS_FILTER (Fig. 1) for modeling the behavior of a LPF shown in Fig. 5. The proposed LPF model is composed by an *entity* and an *architecture*, where bold text indicates reserved words and uppercase text indicates predefined concepts. The entity declares the generic model parameters and specifies two interface terminals of nature electrical. The parameters are set with specific numerical values for a sample filter. The proposed LPF model includes the following electrical terminals: input – i (or in) and output – o (or out). The architecture of the model contains Laplace transfer function provided by the 'ltf attribute.

```
library ieee;
use ieee.electrical_systems.all;
entity LOWPASS_FILTER is
  generic (
    tau1   : real := 10.0e-6;
    tau2   : real := 1.0e-6;
     H0    : real := 1.0);
  port (terminal i  : ELECTRICAL;  terminal o : ELECTRICAL);
end entity LOWPASS_FILTER;
architecture arch_lpf of LOWPASS_FILTER is
  quantity vin across i to ELECTRICAL_REF;
  quantity vout across iout through o to ELECTRICAL_REF;
  constant num : REAL_VECTOR := (1.0, tau2);
  constant den : REAL_VECTOR:= (1.0, tau1);
begin
  vout == H0 * vin'ltf(num, den);
end architecture arch_lpf;
```

Fig. 5. A LPF behavioral VHDL-AMS model.

D. A hierarchical block for modeling of a programmable frequency divider

A block for modeling of a programmable frequency divider is created for simulation modeling of frequency synthesizers. A specific feature is that the coefficient *N* is defined as an external parameter and *N* can be set with the arbitrary integer value. The VHDL description of the model is shown on Fig. 6.

The proposed divider model includes two input terminals (input clock signal – clk and input- reset – reset) and one output terminal cout of std_logic type.

At high logic level of the reset the divider is reset. In the architecture of the model is defined a process by which the frequency division is controlled. By incrementing the count the rising and falling fronts of the input clock signal clk are counted. When reaching the specified value of the parameter *N*, the output signal is obtained. The output signal has a period corresponding to the division ratio.

```
library ieee;
 use ieee.std_logic_1164.all;
 use ieee.std_logic_unsigned.all;
.....
     process (clk, reset)
          begin
          if (reset = '1') then
             count <= 0;
             clkin <= '0';
          elsif rising_edge(clk) or falling_edge(clk) then
                if (count >= N-1) then
                 clkin <= not clkin;
                 count <= 0;
              else
                count <= count + 1;
         end if;
         end if;
        end process;
.....
```

Fig. 6. A part of the frequency divider behavioral VHDL-AMS model.

Examples for modeling of DPLL ICs

The verification check of the proposed behavioral model is performed by doing comparative analysis with simulation results and experimental test of the breadboard circuits with the monolithic DPLL CD74HC4046 (biased with $+5V$ power supply) from Texas Instruments. The simulation modeling is implemented within programming system SystemVision (version 5.5, Mentor Graphics) [15]. After implementation of the computer simulations, experimental study on various circuits of DPLLs was performed. The tested DPLLs were implemented on a FR4 PCB laminate with SMD passive components.

For building the model of IC CD74HC4046 is accepted, that it will work at a center frequency of a VCO equal to $f_0 = 10kHz$ at $U_{ctrl} = 2{,}5V$, a maximum operating frequency $f_{\max} = 15kHz$ within the lock range, settling time $t_{set} = 200\mu s$ at $\leq 0{,}5\%$, overshoot equal to $\leq 20\%$ and supply voltage $+5V$.

According to the datasheet [16] is found that $R_1 = 10k\Omega$ and $C_1 = 47nF$ at $f_0 = 10kHz$ and $V_{CC} = +5V$. The value of the time constant is calculated $\tau' = R_1.C_1 = 470\mu s$ and according to the datasheet is obtained $2f_L = 10kHz$ (or $f_L = 5kHz$), as $f_{\min} = f_{\max} - 2f_L = 5kHz$. Then for the coefficients of the VCO and PD is obtained $K_0 = 19{,}7.10^3 r/s/V$ and $K_p = 0{,}8V/rad$, as well for the parameters of the LPF – $C_2 = 470nF$, $R_3 = 2{,}15k\Omega \pm 1\%$ and $R_4 = 499\Omega \pm 1\%$ ($\xi = 0{,}45$ and $\omega_n = 2{,}5.10^3 r/s$). The parameters C_2, R_3 and R_4 corresponds to the C, R_1 and R_2 on Fig. 1, respectively. According to [8] for the output stage of PD are set the following parameters: $KP = 40\mu A/V^2$; $W = 32\mu m$; $L = 2\mu m$ and $VTON = -VTOP = 2{,}5V$. Based on the values of C_2, R_3 and R_4 for the time constants of the block modeling of the LPF are obtained $tau1 = 1{,}26ms$ and $tau2 = 0{,}23ms$. Then the verification check of the efficiency of the proposed model is performed. At a frequency $f_0 = 10kHz$ after completion of a simulation a control voltage $U_{ctrl0} = 2{,}51V$ is determined and trough the experimental test with CD74HC4046 is found $U_{ctrl0} = 2{,}55V$. After that at frequency $f_{\min} = 5kHz$ are obtained $1{,}11V_{sim.}$ and $1{,}08V_{meas.}$, respectively. A maximum operating frequency of the VCO approximately equal to $30kHz$, as for it are found $4{,}46V_{sim.}$ and $4{,}41V_{meas.}$. Furthermore, the value of the frequency lock range is $2f_L = 10{,}36Hz$. This value is very close to the data given in the datasheet ($2f_L = 10kHz$).

Similar checks are performed at two values of the center frequency – $100kHz$ ($K_0 = 196{,}3.10^3 r/s/V$; $tau1 = 125{,}4\mu s$; $tau2 = 23{,}2\mu s$) and $1MHz$

($K_0 = 2{,}55.10^6 r/s/V$; $tau1 = 1{,}63ms$; $tau2 = 35\mu s$). The corresponding values of the $2f_L$ equal to $108{,}7kHz$ and $1{,}096MHz$. The value of the relative error is not higher than 10% (as a concrete for the three cases are obtained 3,6%, 8,7% and 9,6%, respectively). These simulation results guarantee the workability of the proposed DPLL model and the accuracy of the corresponding mathematical description.

A validation check of the proposed DPLL model is performed by comparison analysis between simulation results and physical test of a frequency synthesizer circuit implemented by IC CD74HC4046 and programmable frequency divider connected within negative feedback network of the PLL. The frequency divider is realized by using microcontroller MSP430G2553. The parameter N is 9-bit binary number, which is set by 10 contacts DIP switch. The DIP switch is connected to pins 8, 13, 14, 15, 19, 20, 16, 17 and 18 of the microcontroller. The test input signals generated from a standard pulse generator model HP8112A. Moreover the input signals are with amplitude $5V$, frequency 10kHz and a duty cycle equal to 50%. The forms of the input and output signals are analyzed with two-channel digital oscilloscope type TDS1012B. For measuring of the frequency of the input and output signal is used frequency counter, model GFC-8010H.

The VCO output frequencies obtained by simulation and the physical experiments are presented on Fig. 7. It is seen that the responses are very close. The maximum error is not higher than 3%.

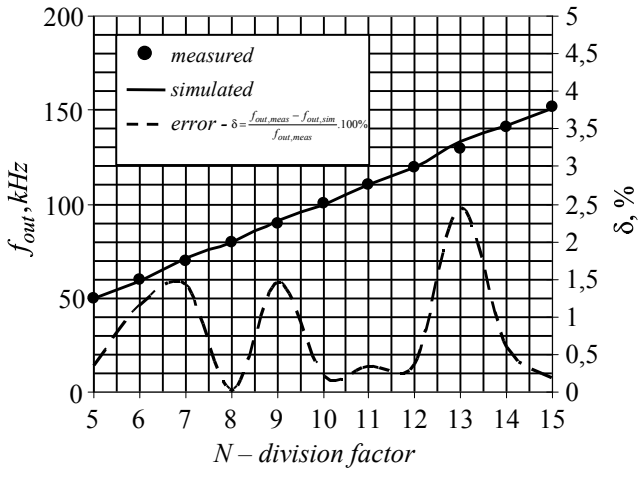

Fig. 7. Response data for the programmable frequency synthesizer.

Conclusion

In this paper a generalized behavioral VHDL-AMS model of monolithic DPLL, based on the data sheet characteristics, has been presented. The model is implemented as a hierarchical structure of blocks representing the basic elements of the DPLLs. For design and modeling of DPLL based frequency synthesizers a behavioral model of a programmable frequency divider is created.

The workability of the created model was proved by comparison of simulation results, with the data sheet parameters and the results of the experimental study of the breadboard circuits with monolithic DPLL CD74HC4046 from Texas Instruments.

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