Performance investigation of deep and ultra-deep submicron CMOS transistors in analog circuit design

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The article discusses the procedure for examination the performance of deep and ultra-deep submicron CMOS transistors with application in analog integrated circuit design. The study is illustrated by using BSIM4 model of 45nm bulk CMOS technology, but presented methodology can be applied to any CMOS technology. At first, simulation experiments and graphical approaches for determination the boundaries of the three basic regions of operation and the key performance parameters – intrinsic gain, unity-gain frequency and supply current are presented. The dependencies of the considered performance parameters from biasing of the transistors and channel length are investigated and visualized. The results are analyzed and qualitative tables that support the selection of the appropriate values of biasing voltage and channel length in the initial stage of analog design are created. The described procedure can be applied to characterize the performance of new unknown deep and ultra-deep submicron CMOS technologies.

Изследване на CMOS транзистори от дълбоки и свръх-дълбоки субмикронни технологии при проектиране на аналогови интегрални схеми (Емил Д. Манолов). *В статията се разглежда процедура за изследване на характеристиките на CMOS транзистори от дълбоки и свръх-дълбоки субмикронни технологии при проектиране на аналогови интегрални схеми. Изучаването е онагледено с помощта на BSIM4 модел на 45nm CMOS технология, но представената методология може да бъде приложена към всяка CMOS технология. Най-напред са разгледани симулационни експерименти и графични подходи за определяне на границите на трите основни области на работа и ключовите параметри на функциониране на транзисторите – вътрешното усилване, честотата на единичното усилване и консумирания ток. Изследвани са и са онагледени зависимостите на параметрите на транзисторите от постояннотоковия режим и дължината на канала. Резултатите са анализирани и са обобщени в таблици, които подпомагат избора на подходящи начални стойности на дължината на канала и пренапрежението на транзистора. Представената процедура може да бъде приложена за характеризиране на нови неизследвани дълбоки и свръх-дълбоки субмикронни CMOS технологии.*

Introduction

Increasing the component's density and functionality of the integrated circuits is associated with reduction the channel length of the transistors. For the past 40 years the minimum channel length of transistors in CMOS integrated circuits is reduced from several micrometers to several nanometers [1]. This is presented in Table 1. Currently ultra-deep submicron technologies are most commonly used in the research and development of analog circuit design.

The reduction of the channel length of the CMOS transistors results in significant complication of the procedures of analog circuits design. Deep, ultra-deep submicron and nanometer CMOS technologies are characterized with substantial change in the transistor's behavior [2], [3]. Depending on the applied gate-source voltage U_{gs} the transistors can work in three main operating regions – weak inversion (sub-threshold), strong inversion and velocity saturation (mobility degradation) [4], [5].

Table 1

Evolution of CMOS technologies

Type	Period	Channel length
Micrometer	Up to 1985	Lmin>1 μm
Submicron	1985 - 1995	1μm>Lmin>0.35μm
Deep submicron	1995 - 2003	0.35μm>Lmin>0.1μm
Ultra-deep submicron	2003 - 2014	0.1μm >Lmin>0.01μm
Nanometer	After 2014	Lmin<10nm

The behavior of transistors in each of the regions is radically different. The weak inversion is characterized with low current and low transconductance, which lead to low speed and low noise immunity. The mobility degradation region determines high consumption and is used for the design of high speed circuits. The typical design of analog integrated circuits is performed in strong inversion region, in saturation area. In this region are valid well-known square low relations of the current through the transistor [6], [7]. The reduction of the channel length narrows the strong inversion region and hampers the design procedures.

The first step in the design of analog integrated amplifiers is to determine both design parameters – channel length L and biasing gate-source voltage U_{gs} for each transistor [8]. The goal is to meet the requirements for the bandwidth and the gain of the designed stage. The next step is the calculation of channel width by using well-known formulas [5], [6], [7]. After that, using successive simulations, designer optimizes the mode of operation and the size of transistors. This is an interactive procedure which success depends greatly on the chosen initial values of the design parameters. Hence, it is extremely important designers to have close insight into the performance of the used technology. This will enable them to orient and to choose the most appropriate mode of operation depending on the specifications [9].

The article discusses the procedure for examination of intrinsic gain, bandwidth and supply current of deep and ultra-deep submicron CMOS transistors. These parameters present the key aspects of the transistor performance in analog circuit applications [5], [9]. The intrinsic gain A_u expresses the maximum possible low-frequency small signal voltage gain that transistor with specified dimensions and biasing can provide in saturation. The bandwidth is determined by the unity gain frequency f_u of the studied transistor, operating in saturation. The value of supply current I_d indicates the energy consumption.

The analysis of discussed performance parameters can be carried out on the basis of the well-known equations that describe the operation of the transistor in each of the three regions [4], [5]. Common models applicable to ''all regions of operation'' can be used, also [8]. The disadvantage of these approaches is the lack of visibility and the big error in determining the parameters of the equations, which have different values for different technologies. Another drawback is the strong dependence of the values of the model parameters on the mode of operation and channel length [3], [4], [5]. The mentioned disadvantages lead to the conclusion that in the initial design step would be appropriate to present and select graphically the discussed performance parameters. This approach will provide the actual information related to the specific parameters of the used technology and will simplify determination of initial values of channel length L and gate-source voltage U_{gs}.

The aim of the article is to present simulation experiments and graphical approach for investigation the intrinsic gain, bandwidth and supply current of deep and ultra-deep submicron CMOS transistors. For this purpose, the dependencies of the discussed performance parameters from channel length L and biasing gate-source voltage U_{gs} of the transistor are examined and visualized.

The study is illustrated by using universal BSIM4 model of 45nm bulk nMOS transistor recommended in Predictive Technology Model website [10]. The model is compatible with used LTSpice circuit simulator.

At first are plotted transconductance g_m, intrinsic gain A_u, unity-gain frequency f_u and supply current I_d versus biasing gate-source voltage U_{gs} for nMOS transistor from examined technology. From them, by geometric drawing, are determined the boundaries of the three basic regions of operation. The next step is to compare and analyze the performance and tradeoffs in different regions of operation. Finally, the dependence of performance parameters from channel length L is explored.

The present procedure can be applied to nMOS and pMOS transistors of any CMOS technology.

Examination of basic performance parameters of ultra-deep submicron CMOS versus gate-source biasing voltage

Fig. 1 shows test circuit for examination the dependence of transconductance g_m of 45nm nMOS transistor in saturation from biasing gate-source voltage U_{gs}. The transconductance g_m will be determined by differentiation of the drain current. The same circuit is used to demonstrate supply current I_d, which characteristic coincides with the transfer characteristic of the transistor. Usually, in order to obtain stable characteristics, it is recommended that channel length L have to be selected up to 5÷8 times of the minimal channel length $L_{\min}$ [4], [5]. In presented case the used channel length is $4L_{\min}$.

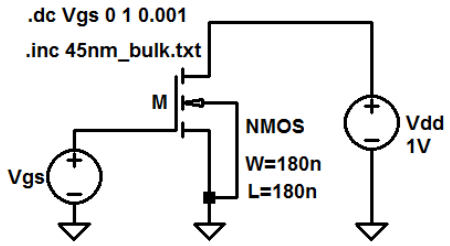

Fig. 1. Test circuit for transconductance g_m examination.

Fig. 2 proposes test circuit for examination of intrinsic gain A_u of the nMOS transistor M from gate-source voltage U_{gs} applied by dc voltage source Vgs [9]. The ac test signal is provided by Vac voltage source.

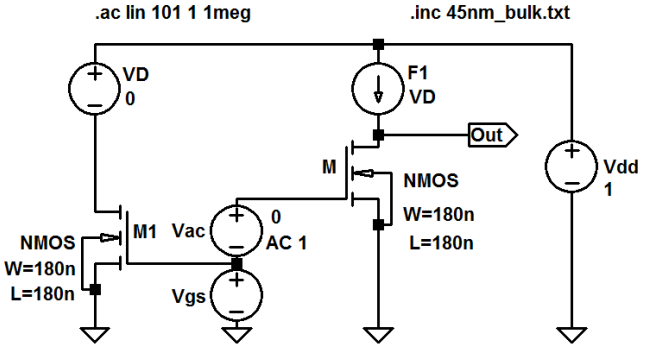

Fig. 2. Test circuit for intrinsic gain Au examination.

The load of the transistor M is the ideal dc current source F1 from the Current Controlled Current Source VD-F1. As a result the gain of the stage depends only on transconductance and output resistance of the examined transistor M. The additional transistor M1 is identical with M and ensures the dc current through the input of the Current Controlled Current Source VD-F1 to be equal to the dc current through M. As the current transfer coefficient of VD-F1 is 1, the currents through F1 and M are equal, which ensures the adequacy of the obtained results. The circuit allows investigation of the intrinsic gain A_u for different dc values of gate-source voltage. To this aim series of ac simulations, one for each value of the dc parameter U_{gs}, have to be carried out.

The test circuit for examination of the bandwidth is presented on Fig. 3 [7]. The circuit allows determination of the unity gain frequency f_u for different values of gate-source voltage. For this purpose, a series of successive simulations for each value of the parameter U_{gs} have to be implemented again.

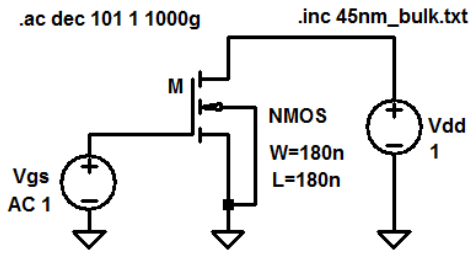

Fig. 3. Circuit for unity gain frequency f_u examination.

Fig. 4 presents the results from investigation of the above discussed parameters for 45nm nMOS transistor with $L = W = 4L_{\min} = 180nm$ and W/L ratio 1. To transform the results for transconductance g_m and supply current I_d to another ratio, it is enough to multiply the presented results by corresponding factor. Unity gain frequency f_u and intrinsic gain A_u practically do not depend on the W/L ratio.

The four plots illustrate the transistor's behavior in the three basic regions of operation: weak inversion (gate-source voltage is below transition point U_{ws}); strong inversion (gate-source voltage is between U_{ws} and transition point U_{sv}) and mobility degradation (from transition point U_{sv} to U_{dd}). The first (lower) plot presents the transconductance vs applied gate-source voltage – $g_m = f(U_{gs})$. The second (above) plot visualizes the results from investigation of intrinsic gain $A_u = f(U_{gs})$. The third plot shows unity gain frequency $f_u = f(U_{gs})$ and the top (four) plot is $I_d = f(U_{gs})$ function.

The boundaries of the regions of operation are determined by using geometric drawing [4, 5]. To this aim an extrapolation of the linear section of the g_m is drawn with straight line. This line intersects U_{gs} axis at point $U_{gs} = U_{th} = 0.42V$, where $g_m = 0$ (U_{th} is threshold voltage). The transition point between weak and strong inversion region U_{ws} is defined as the minimal voltage where the linear section of the g_m curve and the straight line are merged. The upper end of the same line crosses the line that fixes the maximum value of transconductance g_m in mobility degradation region. This intersection defines the transition point $U_{sv} \approx 0.78V$ between strong inversion and mobility degradation. The strong inversion region is among transition point between weak and strong inversion $U_{ws} \approx 0.48V$ and U_{sv} point.

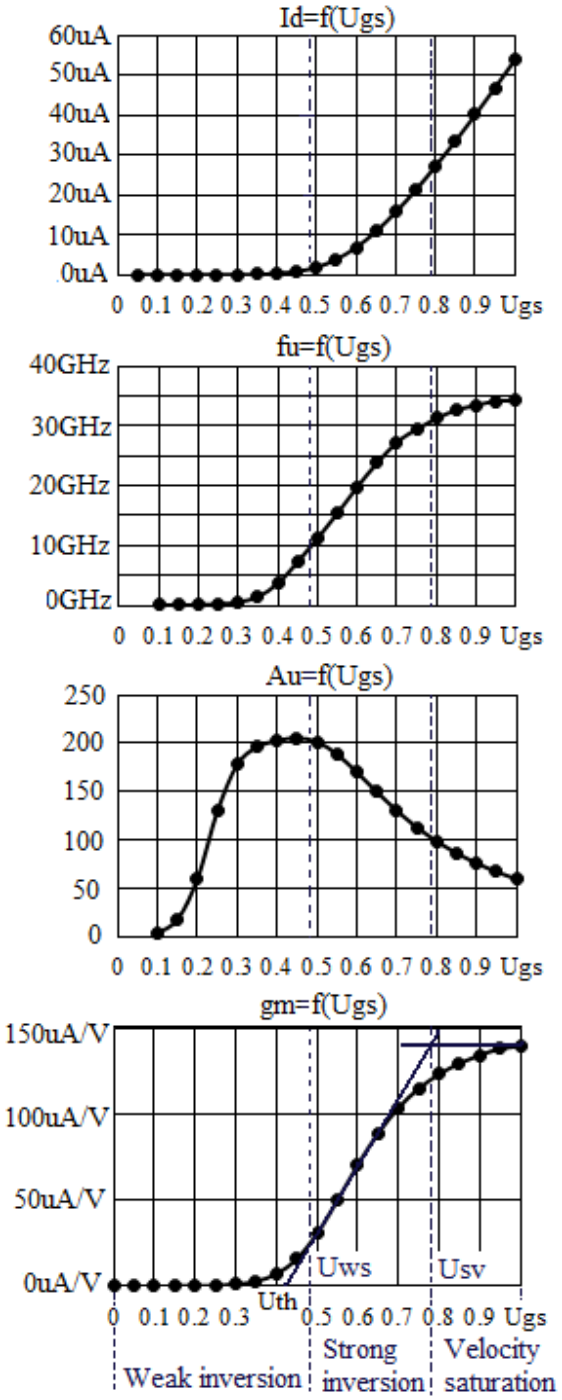

Fig. 4. Results from investigation of basic performance parameters of 45nm bulk nMOS.

The obtained graphical results lead to the following conclusions concerning the investigated technology:

- The higher values of the unity gain frequency (about 35GHz) are in velocity saturation region, but in the same region the intrinsic gain is over 2 times less than its value around U_{ws} transition point. The operation in this region is characterized with high value of supply current (from 25μA up to 50μA), i.e. high power consumption.

- The higher values of the intrinsic gain (about 200) are around transition point U_{ws} between weak and strong inversion, where the supply current has very small values (about several μA). The disadvantage is the reduced (3÷4 times) value of unity-gain frequency.

- Low consumption (smaller than 1μA) with high gain is observed in weak inversion region, at values of gate-source voltage around threshold voltage U_{th}.

Table 2 summarizes the presented conclusions.

Table 2

Qualiative results from examination of 45nm nMOST

	Weak inversion	**Strong inversion**	**Velocity saturation**
Intrinsic gain	High	Medium	Low
Bandwidth	Low	Medium	High
Supply current	Low	Medium	High

The presented table support the selection of appropriate gate-source biasing voltage on the base of specified unity gain frequency and the gain of the designed stage. After, the sizes of the transistors can be refined by interactive simulation based optimization. The described procedure is particularly suitable in initial stages of analog integrated circuit design.

Examination of basic performance parameters of ultra-deep submicron CMOS transistor versus gate-source biasing voltage and channel length

The above presented results are valid for the channel length L equal of $4L_{\min}$. In practice the channel length can be selected from $L_{\min}$, up to $8L_{\min}$ and more. This gives significantly large options to choose the values of design parameters.

Fig. 5 demonstrates the results from examination of 45nm nMOS transistor with channel length $L_{\min}$, $2L_{\min}$, $4L_{\min}$ and $8L_{\min}$.

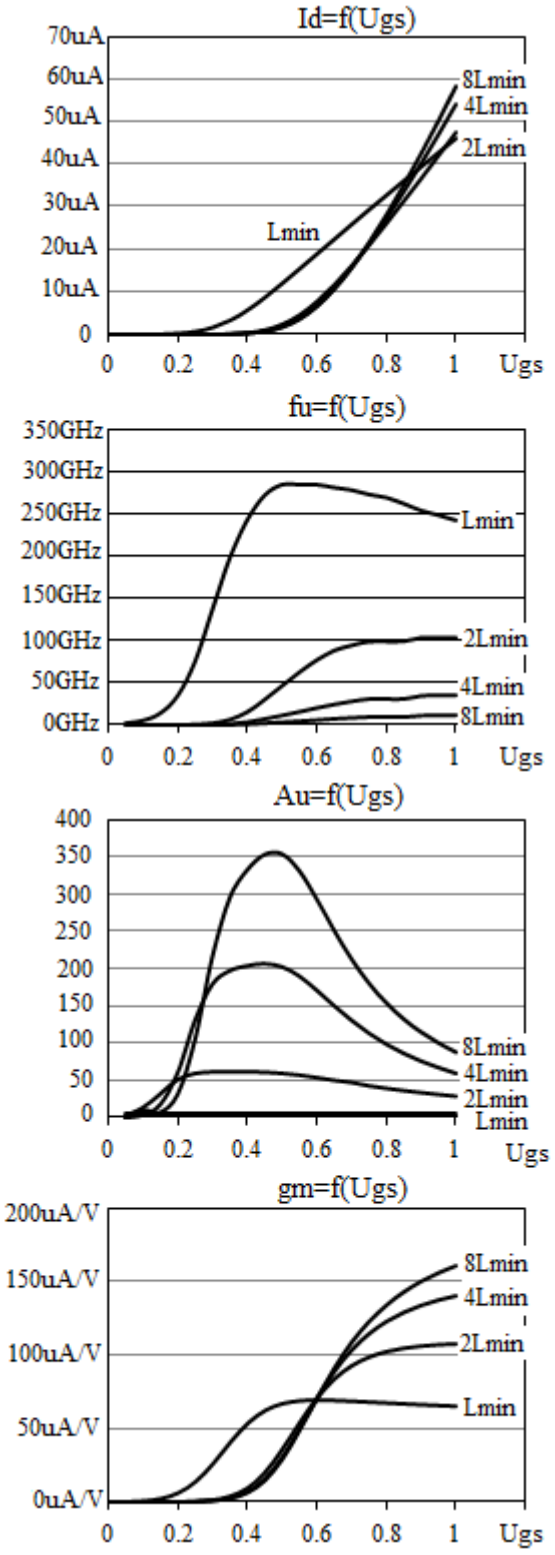

Fig. 5. Investigation of basic performance parameters of 45nm bulk nMOS for different channel length.

As can be seen the increasing of the channel length leads to expansion of strong inversion region. This is particularly evident when comparing transistors with channel length $L = L_{min}$ and $L = 2L_{min}$. For channel length higher than $L = 2L_{min}$ this dependence is less marked. In discussed case the strong inversion region when $L = L_{min}$ is between 0.2÷0.4V; in case of $L = 2L_{min}$ this region is from 0.42V up to 0.7V; at $L = 4L_{min}$ – between 0.46V and 0.76V and for $L = 8L_{min}$ – from 0.5V to 0.82V.

Transistors with a larger channel length have a greater value of intrinsic gain – higher than 350 for $L = 8L_{min}$; over 200 for $L = 4L_{min}$; about 60 for $L = 2L_{min}$ and roughly 5 for $L = L_{min}$.

However, in case of $L = L_{min}$ the examined transistor has unity gain frequency over 250GHz, while for $L = 2L_{min}$ this parameter reduces to 100GHz. At $L = 4L_{min}$ and $L = 8L_{min}$ these values are between 40GHz and 10GHz.

Transistors with $L = L_{min}$ have strong linear transfer characteristic, which determines high supply current in strong inversion. The characteristics for channel length $2L_{min}$, $4L_{min}$ and $8L_{min}$ are quadratic and very close to each other.

The discussed properties of the transistors with different channel lengths are summarized in Table 3. The table illustrates the basic trade-off in analog circuit design – bandwidth vs gain. For high frequency applications can be used transistors with channel length $L = L_{min}$ or $L = 2L_{min}$, but in those cases the gain has very low value. For high value of the gain, channel length has to be large ($L = 8L_{min}$), but then the bandwidth will be very small. The table is appropriate for approximate selection of the channel length in the initial stage of analog design.

Table 3

Qualitative results from examination of 45nm nMOS transistor with different channel lengths

	L=Lmin	**L=2Lmin**	**L=4Lmin**	**L=8Lmin**
Bandwidth	Very High	High	Medium	Low
Intrinsic gain	Very Low	Low	Medium	High

Conclusion

The paper presents procedure for examination of the performance of deep and ultra-deep CMOS submicron transistors with application in analog circuit design. To this aim a set of simulation experiments (Fig. 1, Fig. 2, Fig. 3) are carried out and the obtained results are plotted (Fig.4). By using graphical approaches, the regions of operation of the

examined transistor are determined. The key performance parameters (intrinsic gain A_u, unity gain frequency f_u and supply current I_d) are analyzed and qualitative table that supports selection the appropriate value of biasing voltage is created (Table 2). After, an investigation of dependency of the transistor's performance parameters from channel length is carried out (Fig. 5). The results are summarized and a second qualitative table that ensures the selection of the channel length in the initial stage of analog design is made (Table 3).

The described procedure can be applied when the performance parameters of a new technology are investigated.

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