Power supply circuits for mobile wireless applications

Tihomir S. Brusev

Wireless battery-powered portable electronic devices give opportunity to the people to have faster communication with each other. The increased functionality of mobile phones enables large data packages to be transmitted in the real time. Decreasing of power losses in the electronic building blocks of the transmitter will increase the battery life and system run-time. Power amplifier (PA) is the most energy consuming block. In this paper are considered various power supply circuit architectures suitable for portable electronic devices. Buck dc-dc converter using Pulse-Width Modulation (PWM) designed on CMOS 0.35 µm process is presented. The power losses in the output switching transistors, filter inductor and filter capacitor and evaluated. The efficiency performance of the converter as function of switching frequency f_s and inductor current ripple Δi_L is investigated. The received results show that maximum efficiency can be achieved if Δi_L is twice higher than average output current of the dc-dc converter. Switching-mode dc-dc converters are discussed in terms of applications in the fourth generation Long-Term Evolution (4G LTE) wireless communications standard. Two-phase interleaved buck dc-dc converter is designed on CMOS 0.35 µm technology. The effect of decreased output current ripple compare to single-phase buck dc-dc converter is demonstrated. The received results demonstrate that two-phase dc-dc converters are appropriate choice for LTE applications, when a high frequency envelope signal has to be tracked.

Захранващи схеми за мобилни безжични приложения (Тихомир Брусев). *Преносимите безжични устройства захранвани от батерия дават възможност за по-бърза комуникация между хората. Увеличените функционални способности на мобилните телефони позволяват предаване на големи пакети от данни в реално време. Намаляването на загубите на мощност в изграждащите електронни блокове води до увеличаване на живота на батерията. Мощният усилвател е най-енергоемкия блок в предавателя. В тази статия са разгледани различни захранващи схеми подходящи за преносими електронни устройства. Представена е схема на преобразувател на постоянно напрежение в постоянно (ППН), управляван с широчинно-импулсната модулация (ШИМ), проектирана на CMOS 0.35 µm технология. Изследвани са загубите на мощност в изходните транзистори, филтриращите бобина L и кондензатор C, както и влиянието на честотата на превключване f_s, и амплитудата на променливата съставка на тока протичащ през бобината Δi_L върху коефициента на полезно действие к.п.д. на преобразувателя. Проектиран е двуфазен преобразувател на ППН на CMOS 0.35 µm технология. Демонстриран е ефектът на намаляване на амплитудата на променливата съставка на изходния ток при двуфазния преобразувател, в сравнение с еднофазния. Получените резултати представени в статията показват, че двуфазния преобразувател на ППН е подходящ за LTE приложения.*

Introduction

The rapid development of the telecommunication and the microelectronics technologies in the last twenty years changes substantially the human life. The sizes of the integrated circuits (IC) scale in the range of nanometers [1], [2], [3]. Therefore, large number of transistors could be integrated in the small silicon area, which allows the operation frequencies of the building electronic blocks to be in the range of several GHz [4]. On the other hand increasing of the number of transistor per unit area and frequency of operation of the electronic building blocks leads to increased power consumption of the integrated electronic circuits [5]. Battery-powered portable electronic devices with small sizes and volumes become very popular in the market. The mobile telecommunication devices have developed rapidly. In the nineties and in the beginning of the new century, only voice and text messages could be transferred. Today, except those opportunities, the mobile phones

could be used for high data information transfer [6]. The customers can watch TV programs on their smart phones; they can have fast web browsing; large data packages could be transferred. Different telecommunication technologies have been used during the years. One of the great challenges for the designer remains how to use much more effectively energy from the battery. The costumers have stringent requirements for long operation time of their mobile devices between two recharges of the battery. The lithium-ion batteries, with standard nominal voltage of 3.6 V, are established as the best battery choice for portable telecommunication devices during the years. They have the energy density more than two times higher compare to the nickel-cadmium battery [7]. The tendency in the market of the mobile phones in the beginning of the century has been decreasing of their sizes and volumes [8]. During that time GSM telecommunication standard have been used. Switching-mode dc-dc converters were the choice for power supply circuits, which have to deliver the energy to power amplifier of the transmitter [9]. The advantage of those types of circuits is their high efficiency performance while converting battery voltage to desire output dc voltage level. The efforts of the designers in all over the world were focused on decreasing the size of the whole dc-dc converter system in order to satisfy customer demands [10]. One of the goals has been connected with integration of whole dc-dc converter system, including all the components of the low-pass filter, respectively filter inductor and filter capacitor.

Nowadays mobile phones can perform more and more function, as the new wireless communications standard 4G LTE is appeared. The spectrum is used much more effectively in LTE standard [11]. The customer demands follow the increased functionalities and possibilities of the smart phones. Today the sizes of the mobile electronic devices became larger, which allows increasing of the battery dimensions. Nevertheless, run-time period of the whole system is small and should be increased. New types of power supply circuits, which have to ensure the desire energy of transmitter's power amplifier, have to be used [6]. The standard switching-mode converter cannot fulfill the requirements to deliver appropriate fast dynamically changeable output voltage to drain or collector, respectively of MOS or BJT RF transistor of PA. The aim of this paper is to present the received investigation results of power supply circuits for mobile wireless applications designed on CMOS 0.35 µm technology.

Switching-mode dc-dc converters

Historically, switching-mode dc-dc converters have been a suitable choice for power supply circuits delivering the required voltage to the transmitter's PA of the wireless portable electronic devices. Those types of converter can exhibit theoretically efficiency η of 100% [12], [13]. Due to the power losses in the building circuit's components, the real integrated dc-dc converters can indicate efficiency η values close or greater than 90%. The switching-mode converters have the ability to achieve higher efficiency η compared to linear regulators, especially when the difference between input and output voltage is large [12]. The monolithic buck regulators are in the great interest, because of down scaling tendency in the standard CMOS process technology. In Fig.1 is shown switching mode buck dc-dc converter using PWM control technique.

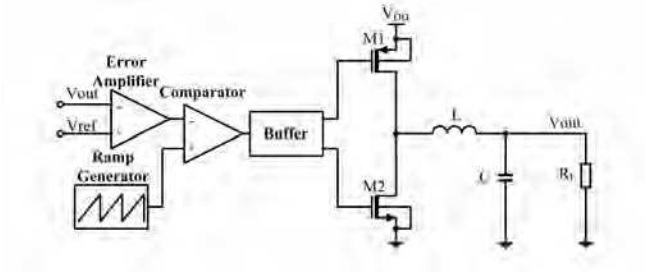

Fig.1. Switching-mode buck dc-dc converter system using PWM control.

The system illustrated in Fig.1 is designed with Cadence on CMOS 0.35 µm process. The power stage of the buck converter includes the output PMOS and NMOS transistors (respectively *M1* and *M2*), filter inductor *L* and filter capacitor *C*. The load resistor R_L represents the current load of transmitter's PA. The control circuit, which performs PWM control of buck dc-dc converter, includes several stages. The stages are respectively error amplifier, ramp generator, comparator and buffer.

Power losses in buck converter

In order to save battery energy and to increase the system run-time of the portable electronic devices, the power losses in the converter's building blocks have to be minimized. The efficiency of the buck converter system can be expressed by:

$$h = \frac{P_{out}}{P_{out} + P_{losses}}, \quad (1)$$

where P_{out} is the output power of the dc-dc converter; P_{losses} are overall power losses in the buck converter system. One of the highest power losses source in the

system are observed in the output MOS transistors *M1* and *M2*. Those losses can be divided into conduction and switching power losses [14]:

$$P_{loss,MOS} = P_{sw} + P_{cond}, \quad (2)$$

The switching losses in turn are equal to [6]:

$$P_{sw} = f_s . C_{tot} . V_{DD}^{\ 2}, \quad (3)$$

where C_{tot} is the input total capacitance of the MOS transistors, f_s is the switching frequency of the buck converter, V_{DD} is the power supply. The conduction losses can be calculated by [14]:

$$P_{cond} = I_{source}^{\ 2} . r_{on,p} + I_{sink}^{\ 2} . r_{on,n}, \quad (4)$$

where I_{source} and I_{sink} are respectively sourcing and sinking current of the MOS transistor, while $r_{on,p}$ and $r_{on,n}$ are on-resistance of PMOS and NMOS transistors. The total power losses in MOS transistor can be further expressed by [15]:

$$P_{tot,MOS} = a\sqrt{\left(I^2 + \frac{\Delta i_L^2}{3}\right) f_s}, \quad (5)$$

where Δi_L is the inductor current ripple, I is a dc current supplied to the load, and a is a coefficient depending from equivalent series resistance of the transistors, C_{tot}, and V_{DD}. The other losses in the buck dc-dc converter are in the filter inductor L. The total power dissipated in filter inductor, assuming that the inductor parasitic impedance scale linearly with the inductance is equal to [15]:

$$P_{ind} = b\left[\frac{I^2}{\Delta i_L f_s} + \frac{\Delta i_L}{3 f_s} + \frac{C_{L0} V_{DD}^2}{R_{L0} \Delta i_L}\right], \quad (6)$$

where b is a coefficient depending on the parasitic capacitance and parasitic series resistance of the filter inductor, C_{L0} and R_{L0} are respectively the parasitic stray capacitance and parasitic series resistance per 1nH inductance. Another contributor of the losses in the power stage of the converter system is the filter capacitor C. Those losses are caused by the effective series resistance of the capacitance R_C. If monolithic capacitor is implemented utilizing the gate oxide capacitance of a MOS transistor, the total power dissipation of filter capacitor is equal to [15]:

$$P_{cap} = d . f_s . \mathrm{D} i_L, \quad (7)$$

where d is a coefficient depending on the technology, effective series resistance of the filter capacitor for MOS transistor with channel width equal to 1µm, gait oxide capacitance, and on channel length of the MOS transistor.

The high f_s is the key parameter, which allows integration of the passive filter components of buck dc-dc converter [12]. The influence of the f_s and Δi_L over the losses in the whole designed system is evaluated below. The supply voltage V_{DD} is chosen to be 3.6 V, which a standard output voltage of lithium-ion battery. The investigations are made when the dc output voltage of the converter is regulated to be 1.3 V. The average value of the output current in this particular case is 22 mA. In Fig.2 is presented the dependence of power losses in the output MOS transistors *M1* and *M2* as a function of f_s and Δi_L. The figure shows that the power losses in the MOS transistors increase with f_s and Δi_L. The reason is that the MOS losses are proportion to f_s and Δi_L, as shown by (5).

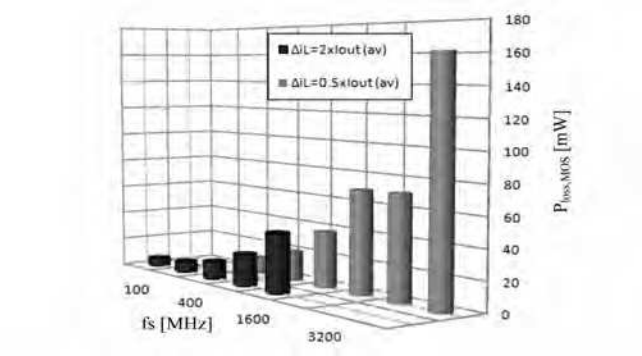

Fig.2. The dependence of power losses in the output MOS transistors M1 and M2 as a function of f_s and Δi_L.

In Fig.3 is presented the dependence of power losses in filter inductor L as a function of f_s and Δi_L. The results are obtained when an off-chip inductor model is used in simulation. As it can be seen from Fig.2 and Fig.3, the power losses in the buck dc-dc converter are mainly determined by the filter inductor at low f_s and Δi_L. With increasing f_s and Δi_L, the inductance value decrease, and thus the dissipation in the parasitic components is lower. On the other hand, the power losses in the MOS transistors go up with increasing f_s. In a particular area of change of the f_s and Δi_L, the power losses in the filter inductor dominate in the buck dc-dc converter. In this region with increasing of f_s and Δi_L, the total power losses in the converter decreases. There is a optimum value of the f_s and Δi_L at which the efficiency of the buck dc-dc converter has a maximum. When the maximum efficiency of buck dc-dc converter is reached, the power losses in the MOS transistors begin to dominate. Further increase of f_s и Δi_L leads to lower converter efficiency. The power losses in the filter capacitor C as function of f_s и Δi_L are presented in

Fig.4. As can be seen, the filter capacitor losses are smaller compare to those in the output MOS transistors and the filter inductor.

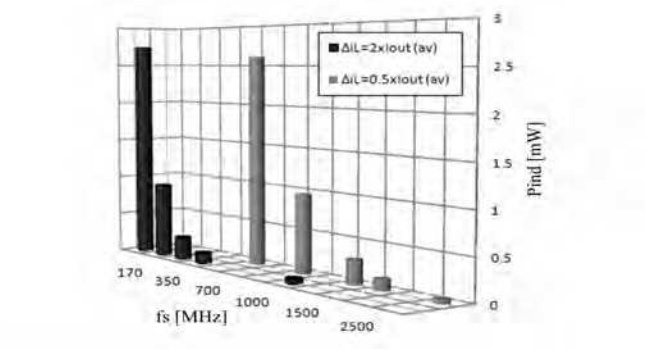

Fig.3. Dependence of power losses in the off-chip filter inductor as a function of f_s and Δi_L.

The power losses P_{cap} goes up with increase of f_s and Δi_L, which is in accordance with the formula (7).

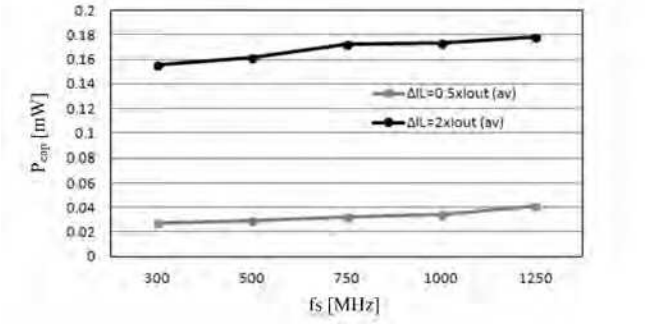

Fig.4. Power losses in the filter capacitor C as a function of f_s u Δi_L.

The design of the PWM control system is focused on the minimization of the current consumption of the different building circuits block. The power losses respectively in the error amplifier, ramp generator, comparator and buffer are considerably small compare to the losses in the power stage.

Efficiency investigation of buck converter

The efficiency of the designed buck dc-dc converter system presented in Fig.1 is investigated below. The output voltage of converter for this analysis is regulated to 1.3V, and then the effect of the f_s and Δi_L is evaluated. The results are presented in Fig.5. The investigations show that maximum efficiency results can be achieved if Δi_L is twice higher than average output current of the dc-dc converter. In this case the circuit operates at the boundary between discontinues and continuous mode. The main transistor in the power stage of the buck converter is switched-on at zero current. Therefore, the power losses are decreased, which improves the overall system efficiency. On the other hand, an increase of f_s, which is desirable for filter's inductor integration, leads to increased switching losses in the output MOS transistors. As can be seen from Fig.5, the efficiency of the buck converter degrades at higher values of f_s.

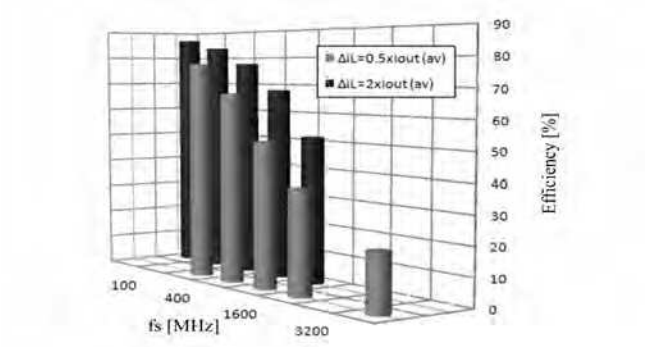

Fig.5. Efficiency of the switching-mode buck dc-dc converter system as function of f_s and Δi_L.

Power supply circuits for LTE applications

Envelope tracking power amplifier system

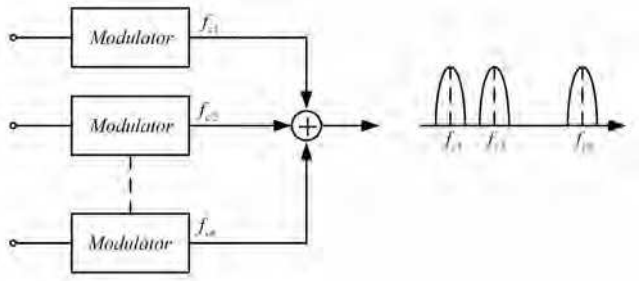

Fig.6. Block circuit diagram of OFDM modulation.

In the LTE standard an orthogonal frequency division multiplexing (OFDM) modulation is used. The information is transferred using several sub-carrier frequencies. Signals with different amplitude and phase are summed in the output of the system [11]. Fig.6 shows a block circuit diagram, which illustrates the basic principles of OFDM modulation. The output signal has big amplitude variation. Therefore in order to prevent distortion of the transmitted information, the power amplifier should be linear. The linearity of transmitter's PA is highly desirable for LTE applications, because it helps to avoid interference with nearby users. The big disadvantage of linear PAs is that those circuits have low efficiency performance. The next important feature of the LTE wireless communication standard is that PAs have to work with very high peak to average power ratio (PAPR) [6]. Therefore in the most of time PA has to work in the back-off mode of

operation. This leads to further unacceptable degradation of the linear PA's efficiency, if constant supply voltage is used. The linear power amplifier consumes equal dc energy for large and low input signal. Its maximum efficiency can be achieved if output power of the PA is high. The efficiency of the PA η_{PA} can be expressed by formula:

$$\eta_{PA} = \frac{P_{out}}{P_{DC}}, \quad (8)$$

where P_{out} is a output RF power of PA, P_{DC} is a dc power delivered to PA. The most promising and used technique for PA's efficiency improvement is envelope tracking [16], [17]. The block diagram of envelope tracking power amplifier (ETPA) system is shown in Fig.7. The envelope amplifier shown in Fig.7 is power supply circuit, which supplies dynamically changeable voltage to the RF transistors of the power amplifier.

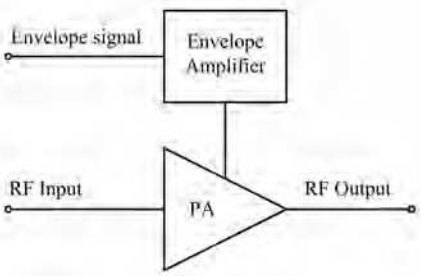

Fig.7. Block diagram of ETPA system.

The envelope amplifier tracks the PA input signal and controls the PA supply voltage according the envelope of this signal. In this way, the output voltage of envelope amplifier is regulated to be close to the envelope of the signal and the overall efficiency $\eta_{ET\,PA}$ of ETPA system is improved. This parameter can be calculated using formula [16]:

$$\eta_{ET\,PA} = \eta_{EA}.\eta_{PA}, \quad (9)$$

where η_{EA} is the efficiency of the envelope amplifier; η_{PA} is respectively the efficiency of the PA.

Hybrid envelope amplifier architectures

In the LTE communication standard envelope amplifier has to have fast tracking speed performance, because envelope frequency is high. The standard PWM controlled switching-mode dc-dc converters, used in GSM application, cannot fulfill this requirement. The f_s of the dc-dc converter have to be to be 5 to 10 times higher than the bandwidth of the LTE signal, if only switching-mode converter is used as an envelope amplifier [18]. In this case the f_s will be at least higher than 100 MHz, which is going to increase to unacceptable values power losses in the converter. The result will be a degradation of the overall efficiency of the ETPA system.

In practice, a hybrid combination between linear amplifier and switching-mode amplifier are used to perform the function of envelope amplifier [6], [11], [14]. The main idea is that a switching-mode amplifier delivers the low-frequency signal content and the dc voltage, while linear amplifier supplies the high frequency signals to the transmitter's PA. In Fig.8 is illustrated a series combined hybrid architecture composed by a switching-mode buck dc-dc converter and a linear amplifier [19]. The linear amplifier in the series combined hybrid envelope amplifiers architectures should filter output ripples generated from buck converter. All the noises coming from envelope amplifier to the PA will be mixed with the transmitted signal, which will results to a distortion of the transferred data. The drawback is that for high f_s the linear amplifier has a low power supply rejection ratio (PSRR) [6]. Also, the entire power delivered to the PA goes through power MOS transistor of the switching-mode amplifier. Therefore switching power losses will be increased especially for high f_s.

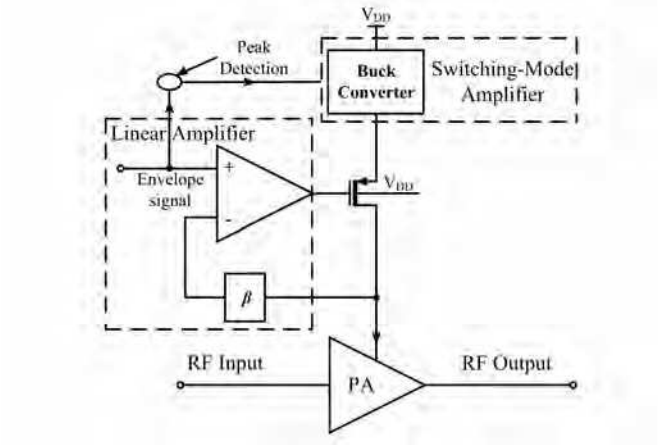

Fig.8. Series combined switching and linear regulator topology of envelope amplifier.

The block circuit of parallel combined hybrid architecture is shown in Fig.9. The switching-mode amplifier is used to deliver average power to PA. The linear amplifier has to deliver the remaining part of the power to PA, when switching regulator cannot respond quickly. The most of the envelope powers have low frequency, which means that the biggest part of the energy is delivered by the high efficient switching-mode stage. This leads to increasing of overall efficiency of the ETPA system. The low efficient linear amplifier delivers only small part,

between 20% and 30%, of the all necessary energy of the PA [20].

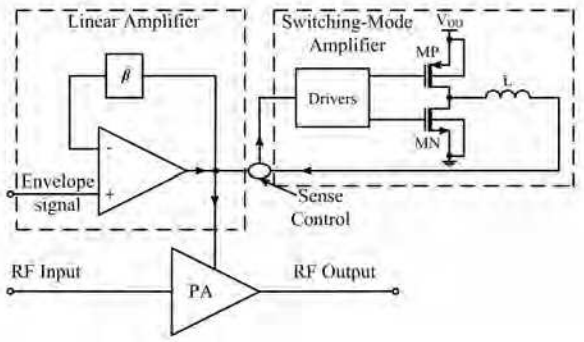

Fig.9. Parallel combined switching and linear regulator topology of envelope amplifier.

Multiphase switching-mode amplifiers

Multiphase switching-mode amplifiers are an alternative of hybrid envelope amplifier used as a power supply circuits for LTE applications. In these architectures low efficient linear amplifier is completely removed. Thus overall efficiency of the ETPA system could be increased. Synchronized adaptive voltage tracking (SAVT) control of two-phased buck dc-dc converter is proposed in [18]. The block circuit diagram of first stage is illustrated in Fig.10.

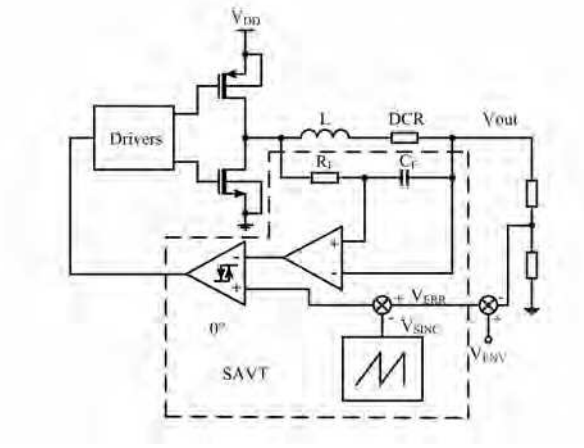

Fig.10. SAVT control of the two-phased interleaved converter [18].

The f_s and the phase of the two sub-converters are synchronized in the implemented hysteresis control in the proposed method. Thus the spectrum of the inevitable switching noises going to power amplifier could be predicted. The two-phased interleaved buck dc-dc converter is designed and investigated on CMOS 0.35 µm process. The block circuit diagram of the switching-mode amplifier's architecture is presented in Fig.11. The analyzed multiphase converter used PWM control technique. The LTE envelope signal is applied to the negative input of the error amplifier, while the output voltage of the two-phased converter is applied to the positive input. The control signals of the main MOS transistors of the both power buck stages are 180° phase shifted. The two-phase converter operates at high switching frequency f_s, equal to 76 MHz. The supply voltage V_{DD} is equal to 3.6 V. Output filter inductors *L1* and *L2* of the both power buck stages are equal to 125 nH. The filter capacitor *C* is equal to 5 pF. The average value of the output voltage of the converter is regulated to be equal to 1.5 V.

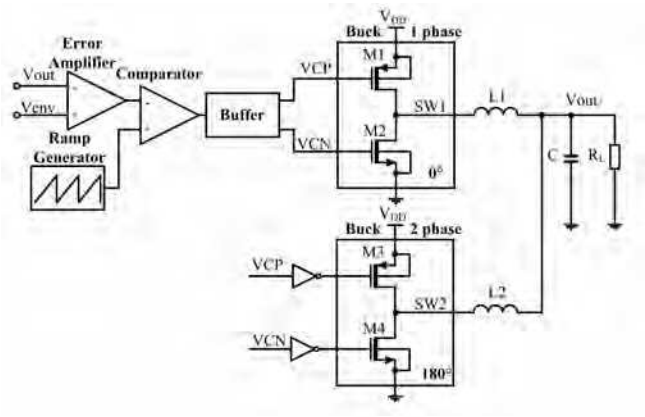

Fig.11. PWM controlled two-phased interleaved buck dc-dc converter designed on CMOS 0.35 µm process.

The load resistance R_L of the two-phase converter represents the current load of RF PA. A source signal with sinusoidal waveform is used in simulations for LTE envelope. The frequency of this sinusoidal signal is equal to 20 MHz. The sinusoidal signal emulates fast changing LTE envelope and it is used in this simulations as a test signal to evaluate the tracking speed of the buck converter. The output voltage signals *VT("SW1")* and *VT("SW2")*, respectively of the first and second buck sub-converter stages are presented in Fig.12. The simulation results demonstrate the synchronization operation in the both sub-converter stages. As it can be seen from the figure, the two voltages are 180° phase sifted. Each sub-converter operates at f_s equal to 76 MHz.

The multiphase dc-dc converter architecture helps for reducing of the output current ripple Δi_{out} of the circuit. The reason is that the phase shifted inductor current ripples Δi_{L1} and Δi_{L2}, respectively of the first and second sub-converter stage, are summed at the output. The output current ripple Δi_{out} of the two-phase buck converter with non-coupled inductors can be expressed by [21]:

(10) $$\Delta i_{out} = \frac{V_{out}}{L}(1-2D)T_s,$$

where D is duty cycle of the converter, T_s is switching period of converter, L is the value of filter inductors (if $L1=L2$, which is the case of the investigated dc-dc converter architecture).

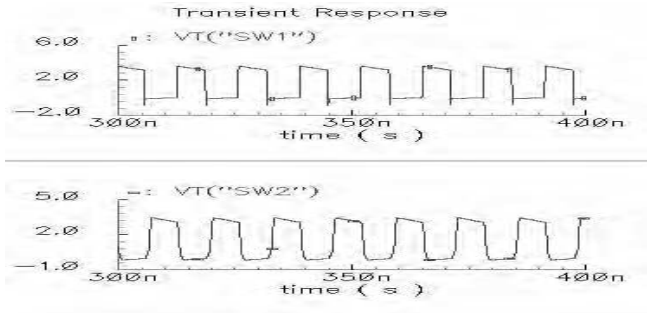

Fig.12. Waveforms of output voltage signals VT("SW1") and VT("SW2").

According to (10) minimum values of Δi_{out} can be received if duty cycle of the converter D is close to 0.5. The inductor current ripples Δi_L of the single-phase and two-phase interleaved buck converter with non-coupled inductors have equal values, and can be expressed by [21]:

(11) $$\Delta i_L = \frac{V_{out}}{L}(1-D)T_s,$$

The waveforms respectively of Δi_{L1}, Δi_{L2} and Δi_{out} of two-phase converter are presented in Fig. 13.

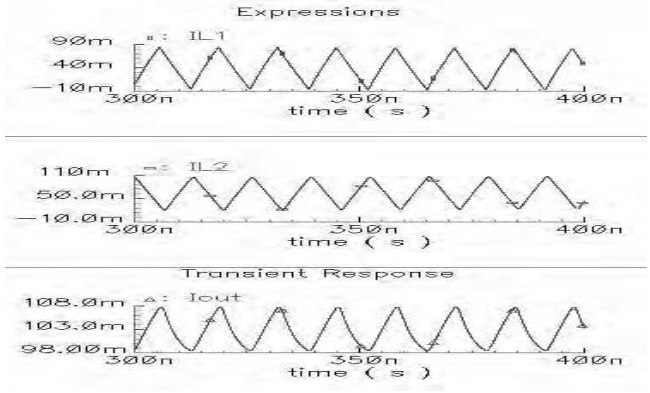

Fig.13. Waveforms of Δi_{L1}, Δi_{L2}; and Δi_{out} of two-phase buck dc-dc converter.

The investigations are made when the average value of the output voltage of the two-phase converter is equal to 1.5 V. The obtained results show that: Δi_{L1} is equal to 88.4 mA; Δi_{L2} is equal to 83.14 mA, and Δi_{out} is equal to 9.2 mA. The average value of the output current of the two-phase buck dc-dc converter is equal to 100 mA. The results show that Δi_{out} is decreased around 9 times than Δi_{L1} and Δi_{L2}, for these particular output parameters of the designed two-phase converter.

Table 1

buck converter	Eff. [%]	$I_{out(av)}$ [mA]	Δi_{out} [mA]	ΔV_{out} [mV]	P_{PMOS} [mW]	P_{NMOS} [mW]
single phase	71	50	9.2	308	3.78	11
two-phase	70.9	100	9.2	132	4.1	10.9

Table 1 presents the obtained simulation results of a single-phase and two-phase buck converters investigated at equal conditions. The values of filter inductors of two circuits are equal to 125 nH, the filter capacitors are equal to 5 pF, f_s is equal to 76 MHz. The average values of the output voltages of the converters are equal to 1.5 V. The average value of load current of the two-phased dc-dc converter is two times higher than the single-phase circuit. The simulations show that Δi_{out} of the two converters have equal values, while output voltage ripple ΔV_{out} of single-phase converter is more than twice higher than ΔV_{out} of two-phase converter. Ideally, the ratio could be even higher if the two-phase converter operates near D=0.5. If the single-phase converter should deliver the same output voltage ripples, the output capacitance C should be significantly increased, which would impact negatively the tracking speed of the converter. If a reduction of tracking speed is not acceptable, the large ripples should be compensated by a linear amplifier, which on the other hand would degrade system efficiency.

Conclusion

In this paper are considered different power supply circuit's architectures suitable for portable electronic devices. PWM controlled buck dc-dc converter designed on CMOS 0.35 µm process is presented. The power losses in the output switching transistors, filter inductor and capacitor and evaluated. Efficiency performance of the converter as function of f_s and Δi_L is investigated. The obtained results show that maximum efficiency is achieved when Δi_L is twice higher than average output current of the dc-dc converter. A two-phase buck dc-dc converter is designed on CMOS 0.35 µm technology. The effect of decreased Δi_{out} compared to single-phase converter is demonstrated. The results demonstrate that two-phase dc-dc converters are appropriate choice for LTE applications, when a high frequency envelope signal has to be tracked.

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