Overview of frequency compensations in the CMOS operational amplifiers, Part two – Advance solutions

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An overview of several common used frequency compensations in the CMOS operational amplifiers is presented. The advantages and disadvantages for each of them are given based on mathematical analysis. Practical circuit examples are shown as well. The work is divided in two parts. The first one explains the need of frequency compensation in the operational amplifiers and demonstrates the simplest possible implementations. The second part describes advance solutions suitable for special cases, where the common used technics do not work, or have low performance. The comparison of all frequency compensations presented in the paper is summarized together with some advises for their use.

Обзор на честотните компенсации в CMOS операционни усилватели, Част втора – Специфични решения (Георги Панов). *Статията представя обзор на най-често използваните честотни компенсации в операционните усилватели направени с CMOS технология. Предимствата и недостатъците на всяка една една от тях са показани като резултат от математически анализ. Дадени са също така практически примери на реализацията им. Работата е разделена на две части. Първата обяснява нуждата от честотна компенсация на операционните усилватели и представя основните схеми. Във втората част са показани решения подходящи за определени случаи, в които класическите методи не работят или дават незадоволителни резултати. Статията завършва със сравнение на разгледаните честотни компенсации и съвети за тяхното използване.*

Introduction

The simplest frequency compensation techniques for the CMOS operational amplifiers (OpAmps) were presented in the first part of the paper. Now, the second part describes advance solutions, which allow better performance in some cases.

Two-stage OpAmp with -40dB/decade slope of the gain

Often (for example in RC filter design) a certain open loop gain at given frequency is needed from the OpAmp. The further run of the gain is not important, only the stability must be assured. It is beneficial to use in this case an OpAmp with gain like in Fig.1, where such an OpAmp is compared with a second one using MFC.

Both OpAmps have the same gain at frequency *Fmax*, but the unity-GBW of the OpAmp with MFC is much larger and hence it is more difficult to ensure its stability.

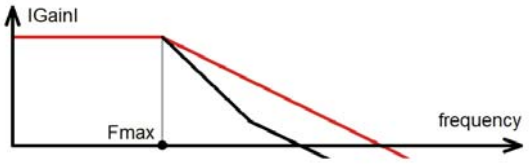

Fig.1. Bode magnitude plots of OpAmp with MFC and OpAmp with -40dB/decade slope of the gain.

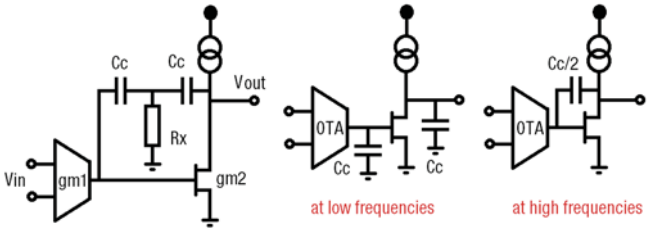

Fig.2. Two-stage OpAmp with -40dB/decade slope of the gain.

The idea of this frequency compensation is, that the Miller capacitor is needed only at frequencies in the range of the unity-GBW [1]. It is shown in Fig.2. The resistor *Rx* breaks the MFC at low frequencies. At

higher frequencies the impedance of the capacitors decreases and the MFC starts to work. The OpAmp has the same DC gain and non-dominant pole like an OpAmp with MFC, unity - GBW = *gm1*/(*Cc/2*), positive zero = *gm2*/(*Cc/2*), negative zero = -1/(2**Cc*Rx*) and two dominant complex poles. The positive zero can be removed using nulling resistor. Gain peaking is possible due to the complex poles. Compared with the MFC, 4 times larger compensation capacitor is needed for the same unity-GBW. Therefore, this frequency compensation is advantageous, if a low-power circuit is desired and more chip area can be spent.

OpAmp with N+1 poles and N zeros in the GBW

Fig.3 shows the simplest implementation of this frequency compensation - only one additional pole/zero pair. Here, -40dB/decade slope of the gain is achieved by using composite first stage: a low frequency path (it conducts until the capacitor *Cx* breaks it) is added in parallel to the first stage (*gmC*) of an OpAmp with MFC.

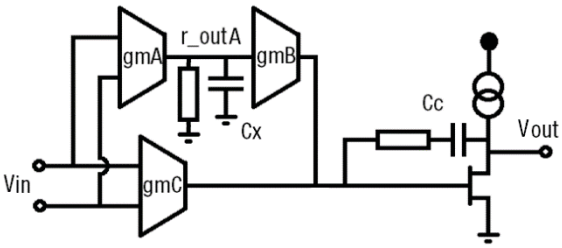

Fig.3. OpAmp with 2 poles and zero in the GBW.

The transfer function can be easily derived from the transfer function of MFC when *gm1* is replaced with *gmC+gmA*r_outA*gmB*/(1+*s*r_outA*Cx*), where *r_outA* is the output resistance of the gmA-stage. There are additionally to the poles and the zero of the Miller compensation a dominant pole = −1/(*Cx*r_outA*) and a zero = −*gmA*gmB* /(*gmC*Cx*) − 1/(*Cx*r_outA*). The unity-GBW is approximately *gmC/Cc*. Such an OpAmp can be built using more pole/zero pairs to achieve very high gain at low frequency [2]. The capacitor *Cx* cannot be connected to the output of the gmB-stage to use the Miller effect, because this will lower the output impedance of the first stage for high frequencies and disturb the operation of the MFC of the whole amplifier.

Two-stage OpAmp with cascoded Miller frequency compensation

Often, an OpAmp has to drive resistive load connected to ground. An OpAmp with MFC as shown in Fig.*4a* is the simplest solution. However, this circuit suffers from bad power supply rejection (PSR): At frequencies where the impedance of the compensation capacitor is lower than the output impedance of the first stage, the compensation capacitor shorts the drain and the gate of the output transistor. Thus, a resistor divider between the supply voltage and the output is built as shown in Fig.*4b*.

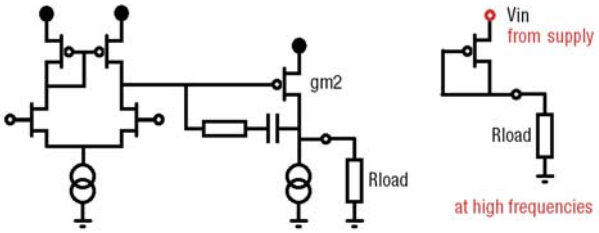

Fig.4. OpAmp driving resistive load to ground
***a.** OpAmp with MFC*
***b.** Behavior of the output stage at high frequencies*

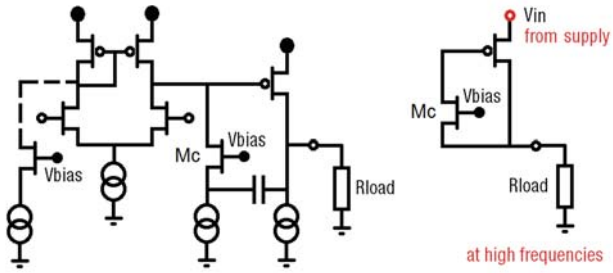

Fig.5. OpAmp driving resistive load to ground
***a.** OpAmp with CMFC*
***b.** Behavior of the output stage at high frequencies*

Cascoded Miller frequency compensation (CMFC) shown in Fig.*5a* can be used to solve this problem [3]. Here the compensation capacitor is not connected directly to the gate of the output transistor, but through cascode connected transistor *Mc*, which separates it from the gate of the output transistor. Now the divider in Fig.*4b* does not exist anymore (Fig.*5b*). The bias voltage on the gate of the cascode transistor *Vbias* must be referred to ground and not to the supply voltage. There is no improvement of the PSR if *Vbias* is referred to the supply voltage. Often, the dashed part in the left is added for symmetry. The circuit in Fig.*5a* does not have positive zero in its transfer function, because there is only one signal path between the outputs of the first- and the second stage. However, this is not true for the CMFC in general. Fig.6 shows a case were the circuit has second path of different type and with opposite sign to the main path. The positive zero cannot be removed with nulling resistor (like in the MFC), because the stability of the inner loop will be degraded. An OpAmp built with folded cascode

OTA with NMOS input pair (Fig.*5a*) has good PSR and no positive zero at the same time. OpAmps using folded cascode OTA with PMOS input pair or telescopic OTA do not have this property.

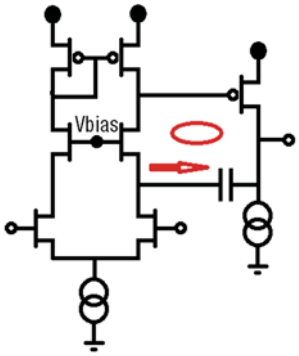

Fig.6. OpAmp with CMFC and positive zero.

The transfer function of OpAmp with CMFC like in Fig.*5a* is:

$$Vout/Vin = gm1*r\_out1*gm2*Rload * [1 + s*(Cc+CgsC)/gmC] / [1 + s*(gm2*Rload*Cc*r\_out1 + Cgs2*r\_out1 + Cload*Rload + Cc*Rload + Cc/gmC + CgsC/gmC) + s^2*(r\_out1*Rload*Cgs2*Cload + r\_out1*Rload*Cgs2*Cc + r\_out1*Cgs2*Cc/gmC + r\_out1*Cgs2*CgsC/gmC + Rload*Cload*Cc/gmC + Rload*Cload*CgsC/gmC + Rload*Cc*CgsC/gmC) + s^3*r\_out1*Rload*(Cload*Cgs2*Cc + Cload*Cgs2*CgsC + Cc*Cgs2*CgsC)/gmC],$$

where *gmC* is the gm of the cascode transistor Mc and *CgsC* is its gate-source capacitance. Commonly it can be simplified to:

$$Vout/Vin = gm1*r\_out1*gm2*Rload* [1 + s*(Cc+CgsC)/gmC] / [1 + s*(gm2*Rload*Cc*r\_out1 + Cgs2*r\_out1 + Cload*Rload) + s^2*r\_out1*Cgs2* (Rload*Cload + Rload*Cc + Cc/gmC) + s^3*r\_out1*Rload*Cload*Cgs2* (Cc+CgsC)/gmC].$$

An OpAmp with CMFC has the same DC gain like an OpAmp with MFC and practically the same dominant pole:

$$\text{dominant pole} = -1/(gm2*Rload*Cc*r\_out1 + Cgs2*r\_out1 + Cload*Rload).$$

There are two non-dominant poles, which can be real or a complex pair. When they are real and significantly different, then the one at lower frequency is (if the output stage has gain and if *Cload* is not an external capacitor in μF range or larger):

$$\text{non-dominant poles} = -gm2*Cc/[Cgs2*(Cload + Cc + Cc/gmC*Rload)].$$

It is usually larger than the non-dominant pole of the MFC. Therefore, the CMFC has more PM than the MFC for the same gm of the output stage. This improvement depends on the ratio between *Cc* and the total capacitance at the input of the output stage *Cgs2*. The PM of the OpAmp is higher, when this ratio is bigger. But moving the pole to higher frequency with larger *Cc*/*Cgs2* changes it together with the other non-dominant pole to become complex. And when their Q-factor is high, it is possible that the inner loop shown in Fig.7 is unstable.

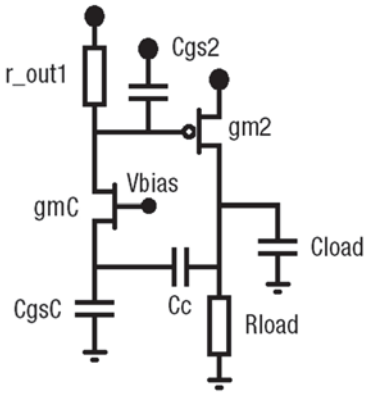

Fig.7.The inner loop in CMFC.

The inner loop has: zero = 0,

$$\text{dominant pole} = -1/(r\_out1*Cgs2)$$

$$\text{dominant pole} = -1/[Rload*(Cload+Cc)+(Cc+CgsC)/gmC]$$

$$\text{non-dominant pole} = -gmC/[CgsC+Cc*Cload/(Cc+Cload)] - 1/[Rload*(Cload+CgsC*Cc/(CgsC+Cc)].$$

Bigger *gmC* improves the stability of the inner loop and at the same time allows to keep the high PM of the CMFC. However, the current consumption increases. Some additional elements can be inserted to assure the stability of the inner loop. Increasing *Cgs2* by adding a capacitor between the gate and the source of the output transistor (Fig.8a) reduces the unity-GBW of the inner loop and improves its stability. But this reduces the PM of the whole amplifier. Adding a capacitor and a resistor in series (parallel frequency compensation) at the same place (Fig.8b) improves

this trade-off. Splitting the compensation capacitor in two equal capacitors as shown in Fig.8c [4] makes the gain of the inner loop always less than 1 and therefore the circuit is stable. Thereby the non-dominant pole of the whole OpAmp is still higher than the one of the MFC. So the power efficiency increases but the advantage of good PSR is lost.

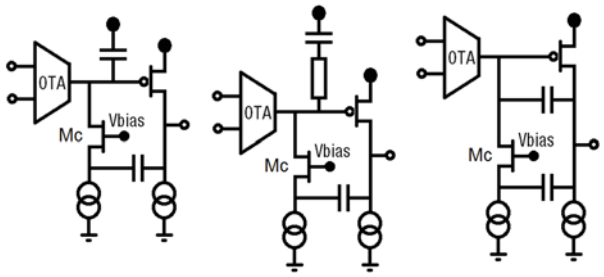

Fig.8. Improving stability of the inner loop in CMFC
***a.** With additional capacitor*
***b.** With additional capacitor and resistor*
***c.** By splitting the compensation capacitor*

Two-stage OpAmp with dominant pole at the output

Some voltage regulators have huge capacitive load permanently connected to the output and can be built as two-stage OpAmp. MFC or CMFC is usually not usable here, because it will require a large current in the output stage in order to have the non-dominant pol at high enough frequency. If the output transistor is small (has small *Cgs2*), then the OpAmp could work without frequency compensation, because the poles at the outputs of the both gain stages are very different. If not, a source follower stage is added between the 1st and the 2nd stages (Fig.9) and the circuit has:

dominant pole = -1/(*Road*Cload*)
non-dominant pole = -1/(*r_out1*C_out1*)
non-dominant pole = -*gmSF*/*Cgs2,*

where *C_out1* is the sum of the output capacitance of the first stage and the input capacitance of the source follower.

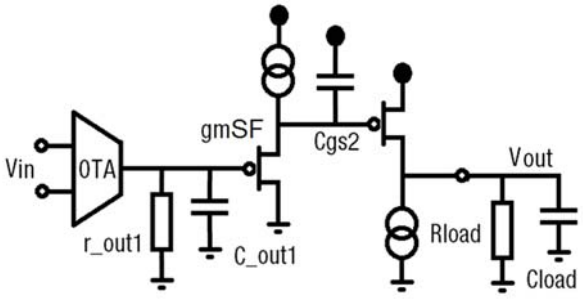

Fig.9. Two-stage OpAmp with dominant pole at the output.

The circuit with source follower stage has two non-dominant poles instead of one, but they are at much higher frequency than 1/(*r_out1*Cgs2*) . It is because the input capacitance of the source follower is less than *Cgs2* and its output resistance is less than *r_out1*.

Two-stage OpAmp for driving variable capacitive load

Sometimes, the OpAmps must drive capacitive loads, which vary hundred or more times. The MFC is not effective in this case, because if the non-dominant pole is canceled with a zero for the case of the maximum capacitive load, the circuit could be instable for the minimum one. This is shown in Fig.10. The reason are high-frequency poles and positive zeros (for example *gm1*/*Cgd1* , where *Cgd1* is the gate-drain capacitance of the input transistors).

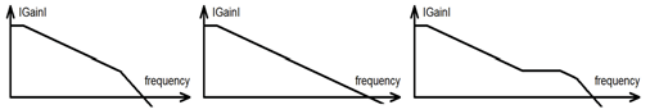

Fig.10. Bode magnitude plot of OpAmp with MFC
***a.** with non-dominant pole inside the GBW and without nulling resistor*
***b.** with non-dominant pole inside the GBW and negative zero equal to the non-dominant pole*
***c.** without non-dominant pole inside the GBW and with negative zero inside the GBW*

A well-known simple technique for driving variable capacitive load is shown in Fig.11. However, it is not suitable for the new low-voltage CMOS technologies due to the voltage drop on the resistor *Ro,* which limits the output voltage range.

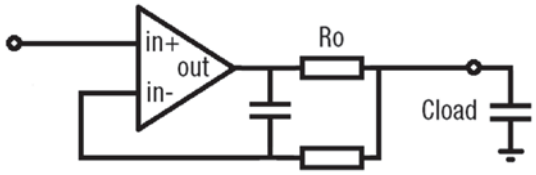

Fig.11. Technique for driving variable capacitive load.

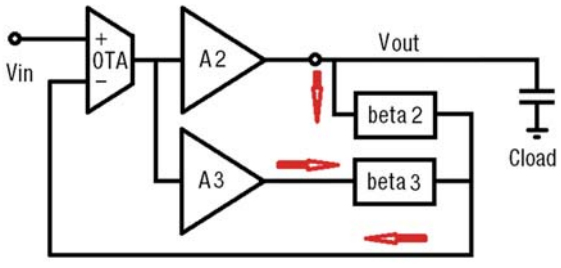

Fig.12. Two-stage OpAmp (with feedback) for driving variable capacitive load.

Fig.12 shows an OpAmp topology, which is capable to drive varying capacitive load with small current consumption [5]. The idea is to have two output stages. The feedback signal to the input at low frequencies comes from the output stage driving the load capacitor. At high frequencies the feedback signal from the other output stage is larger and dominates. This is achieved by making *A3*beta3 > A2*beta2*, where *A2* is the gain of the second stage, *A3* is the gain of the additional stage and *beta* is the corresponding feedback factor. A circuit implementation is shown in Fig.13. The resistor *Rs* is added to set the DC voltage at the output of the additional stage. OpAmps with this frequency compensation suffer from high nonlinearity because of the two feedback paths. Therefore, they are used almost exclusively as voltage regulators.

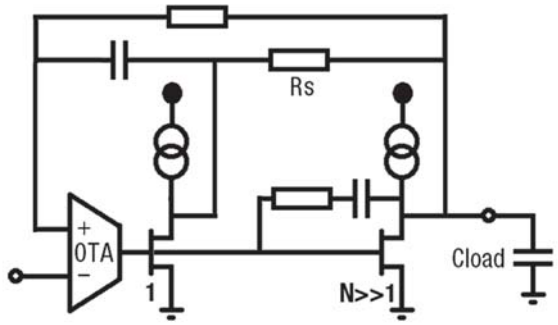

Fig.13. Two-stage OpAmp for driving variable capacitive loads.

Three-stage OpAmp with nested Miller frequency compensation

Sometimes the gain of two stages is not enough to achieve the desired amplifiers open loop gain. One possible solution is to use regulated cascodes [6]. Other one is to use three stages, which is very attractive for circuits working with supply voltage around or below 1V.

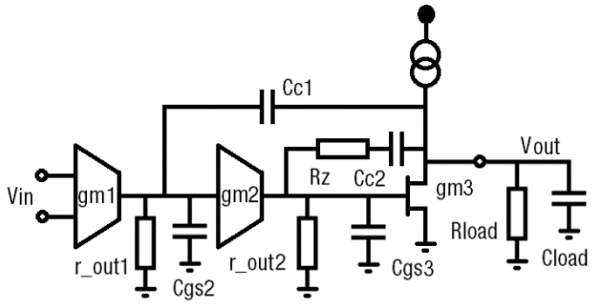

Fig.14. Three-stage OpAmp with nested Miller frequency compensation.

The idea of the nested Miller frequency compensation (NMFC) is the same as of the MFC - to make the transfer function of a three (or more in general) stage OpAmp like this one of the OTA, with only one pole in its GBW. Such an OpAmp is shown in Fig.14. There are two nested two-stage OpAmps with MFC: 1-(2+3) (the whole amplifier) and 2-3 (the inner one). The inner OpAmp works as a buffer for frequency larger than $1/(r\_out1*Cc1)$, if $Cc1 >> Cgs2$ (which is usually the case) and therefore has to be stable with unity gain feedback. The design considerations for the two-stage OpAmp with MFC are valid here. There is no nulling resistor in series with *Cc1* because it will cause a pole in the feedback of the inner amplifier and degrade its stability. The transfer function of the whole OpAmp is:

$$Vout/Vin = gm1*r\_out1*r\_out2*Rload* (gm2*gm3 - s*gm2*Cc2 - s^2*Cc1*Cc2)/ [1 + s*gm2*r\_out2*gm3*Rload* Cc1*r\_out1 + s^2*r\_out1*Cc1*r\_out2* Cc2*Rload*(gm3 -gm2 + 1/Rload) + s^3*r\_out1*r\_out2*Rload* Cload*Cc1*Cc2],$$

when $gm2*r\_out2 >> 1$, *Cload* is not an external capacitor in μF range or larger and $Cc1 >> Cgs2$, $Cc2 >> Cgs3$, which is usually the case.

The dominant pole is $= -1/(gm2*r\_out2*gm3* Rload*Cc1*r\_out1)$

The two non-dominant poles can be real or complex. Their type and positions depend on the ratio between the unity-GBW of the inner OpAmp $gm2/Cc2$ and its non-dominant pole $-gm3/Cload$. Thus, they depend on the stability of the inner amplifier.

If the inner OpAmp is very stable ($gm3/Cload >> gm2/Cc2$), then the non-dominant poles of the whole OpAmp are real and significantly different. The one at lower frequency is $-gm2/Cc2$. The unity-GBW of the whole amplifier must be at least two times smaller (for PM>60 degree) than $gm2/Cc2 << gm3/Cload$. Therefore, in this case NMFC is very power inefficient compared to MFK.

If $gm3/Cload = 2*gm2/Cc2$ (the inner OpAmp has PM about 60 degree), then the non-dominant poles of the whole OpAmp are complex. If its unity-GBW = $gm1/Cc1$ is set to be $0.25*gm3/Cload = 0.5*gm2/Ck2$ then the PM of the whole OpAmp is about 70 degrees. For a given output pole $-gm3/Cload$, the achievable unity-GBW with this frequency compensation is about the half of the one with MFC for the same stability [6].

The transfer function has a positive and a negative zero. The positive one is at lower frequency, which is several times higher than the unity-GBW of the OpAmp, if *gm3* >> *gm2*. Therefore, the impact of the zeros can be usually neglected.

For a given GBW of the whole amplifier, the larger unity-GBW of the inner OpAmp makes the whole amplifier more stable. This leads to interesting property of the NMFC. If the unity-GBW of the whole OpAmp and the pole at the output -*gm3*/*Cload* are fixed, then: reducing the unity-GBW of the inner OpAmp increases the stability of the inner OpAmp and decreases the stability of the whole amplifier. Making the unity-GBW of the inner OpAmp larger increases the stability of the whole amplifier and decreases the stability of the inner OpAmp. The inner amplifier can be compensated with CMFC too, as shown in Fig.15. This allows to increase its GBW for the same *gm3*.

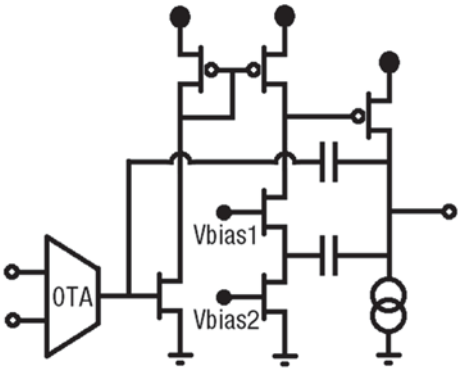

Fig.15. Three-stage OpAmp with NMFC and CMFC.

The NMFC has one disadvantage, which prevents it for use in OpAmps driving low-resistive loads. The unity-GBW of the inner OpAmp has to be larger than the one of the whole amplifier. When the last stage has no gain, the unity-GBW of the inner amplifier decreases and the whole OpAmp could become unstable.

Three-stage OpAmp with multipath nested Miller frequency compensation

The idea of the multipath nested Miller frequency compensation (MNMFC) is to add a zero, which cancels one pole in the GBW [7]. Such an OpAmp is shown in Fig.16. The transfer function is:

$$Vout/Vin = r\_out1*r\_out2*Rload* [gm1*gm2*gm3 + s*(gm3*gmX*Cc1 - gm1*gm2*Cc2) - s^2*Cc1*Cc2* (gm1+gmX)] / [1 + s*gm2*r\_out2*gm3* Rload*Cc1*r\_out1 + s^2*r\_out1*Cc1* r\_out2*Cc2*Rload*(gm3 -gm2 + 1/Rload) + s^3*r\_out1*r\_out2* Rload*Cload*Cc1*Cc2],$$

when *gm1*r_out1* >> 1, *gm2*r_out2* >> 1 and *Cload* is not an external capacitor in μF range or larger. It has the same poles like the one of the NMFC. There is a positive and a negative zero again. However, the negative zero can be placed at frequency smaller than the unity-GBW by proper *gmX*. Thus, one of the two non-dominant poles can be canceled by this zero. Therefore, it is not needed to make both of them bigger than the unity-GBW. In order to do so, the non-dominant poles must be real, which is the case when *gm3*/*Cload* > 4**gm2*/*Ck2*. The non-dominant pole not canceled by the zero has to be at as high frequency as possible.

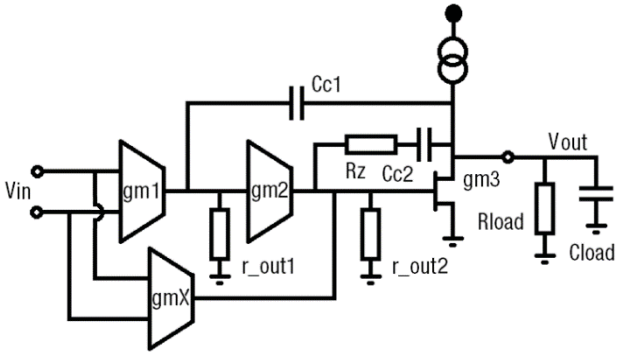

Fig.16. Three-stage OpAmp with multipath nested Miller frequency compensation.

As mentioned in the section for NMFC, when the inner OpAmp is very stable (*gm3*/*Cload* >> *gm2*/*Cc2*), the poles are significantly different and are -*gm2*/*Cc2* and -*gm3*/*Cload*. The negative zero is -*gm1*gm2*/(*gmX*Cc1*) and if *gm1*/*gmX* = *Cc1*/*Cc2*, then it cancels the non-dominant pole at lower frequency.

It is easy to track both frequencies, as *gm1*, *gm0* and *Cc1*, *Cc2* match. Therefore, a doublet increasing the settling time of the OpAmp can be avoided [8].

The remaining non-dominant pole is *gm3*/*Cload*, the same as in the MFC and the unity-GBW of the whole OpAmp can be set to a frequency, like for MFC. Therefore, it is about two times larger than the unity-GBW of OpAmp with NMFC for the same output pole -*gm3*/*Cload* and stability. The inner OpAmp built with the stages 2 and 3 do not need to have larger unity-GBW than the whole amplifier. Thus, this topology can be used in OpAmps driving low-resistive loads.

A simple implementation of OpAmp with MNMFC is shown in Fig.17. Here gmX =

*gm1*gm2*/(2**gmN*). The ratio *gm2*/*gmN* varies with the process and if the matching between the pole and the zero is not good enough, *gmX* has to be implemented as additional input stage.

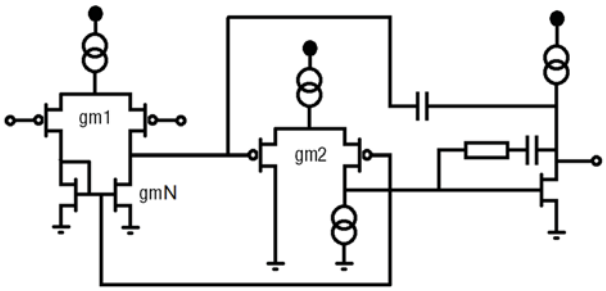

Fig.17.Three-stage OpAmp with MNMFC.

Three-stage OpAmp with nested Miller frequency compensation with feedforward path

This frequency compensation is shown in Fig.18 [9]. There is a non-dominant pole in the GBW of the OpAmp and zero to compensate it, similarly to the MNMFC. The transfer function is:

$$Vout/Vin = gm1*r\_out1*Rload*[gm0*gm2*r\_out2 + gm3 + s*Cc2*r\_out2*(gm3 - gm2) - s*Cc1 - s^2*Cc1*Cc2*r\_out2] / [1 + s*Rload*(gm0*gm2*r\_out2*Cc1*r\_out1 + gm3*Cc1*r\_out1 + Cload) + s^2*r\_out1*Cc1*r\_out2*Cc2*(gm3*Rload + 1 + gm0*Rload - gm2*Rload) + s^2*Cload*Rload*(Cc1*r\_out1 + Cc2*r\_out2) + s^3*r\_out1*r\_out2*Rload*Cload*Cc1*Cc2].$$

When *Cload* is not an external capacitor in µF range or larger, the unity-GBW of the OpAmp is *gm1*/*Cc1*. There are two zeros with opposite signs. The one at lower frequency is negative and depends on the gm of the output transistors. The non-dominant pole at lower frequency (which is in the GBW of the OpAmp) depends on the load capacitor. Therefore, it is impossible to make a practical pole-zero cancelation as in the MNMFC. However, the nested Miller frequency compensation with feedforward path (NMFCFP) has one important advantage. Its high frequency non-dominant pole depends on the sum *gm0* + *gm3*, which allows to place this pole at about two times higher frequency, like in an OpAmp with class AB output stage.

The design procedure of NMFCFP could be as following: There is a two-stage amplifier consisting of stages 1 and 3 (Fig.18) and a three-stage amplifier consisting of 1, 2 and 0. The outputs of the both amplifiers are added at the output of the whole OpAmp. The gain of the three-stage amplifier is larger and therefore it dominates at (at least) low-frequencies.

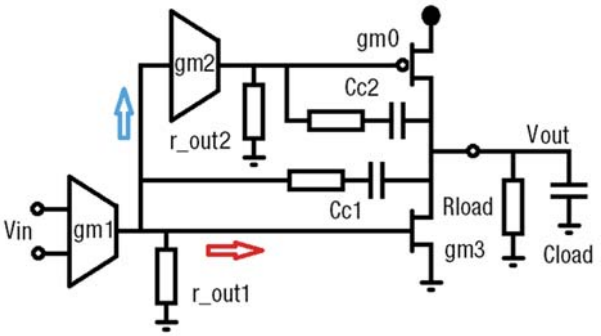

Fig.18. Three-stage OpAmp with nested Miller frequency compensation with feedforward path.

The two-stage OpAmp is easier to make stable, therefore it has to dominate at higher frequency. The first stage and the compensation capacitor *Cc1* are common parts of the both amplifiers. The transfer function from the input of stage 3 to its output is *gm3*Rload*/(*1+s*Cload*Rload*). Its unity-GBW is *gm3*/*Cload*. Stages 2 and 0 forms an OpAmp with MFC. If its GBW *gm2*/*Cc2* is smaller than the unity-GBW of the stage 3, then the two-stage amplifier has more gain at higher frequency and its stability determinates the stability of the whole OpAmp.

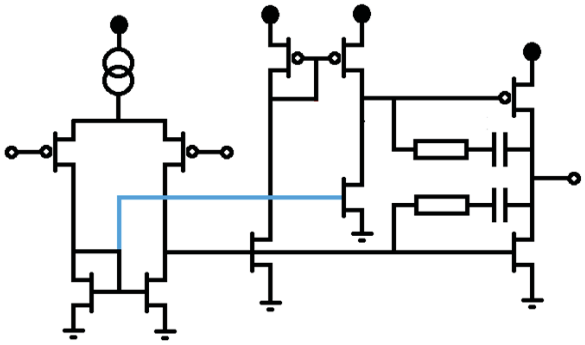

Fig.19. Three-stage OpAmp with NMFCFP.

The amplifier built with stages 2 and 0 can be compensated with CMFC instead of MFC to achieve higher PSR. Fig.19 shows the simplest implementation of OpAmp with NMFCFP, requiring only one bias current. The dependency of the current through the output transistors on the load current is shown in Fig.20a. It is not like in a real class AB stage (Fig.20b [10]). If the load current flows in the OpAmp and is larger than the NMOS quiescent current, then the current through the PMOS drops to zero and the